

# Switched Current Circuits

## Design, Optimization and Applications

by

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*A thesis submitted in the partial fulfilment of the requirements for the degree:  
Doctor of Philosophy (Ph.d)*

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September 4, 1995

# Preface

This thesis is the result of the research I did on Switched Current Circuits. The work was carried out, at the Electronics Institute at the Technical University of Denmark, in the period September 1, 1992 to February 28, 1995.

This thesis consists of 17 chapters grouped into four major parts: Theory, Applications, Appendices and Publications.

The Theory part treats both basic and advanced topics of switched current circuits. In this part we show how basic sampled data systems can be build using Switched Capacitor (SC) and Switched Current (SI) techniques. We also identify the limiting factors in SI circuits and show how to design enhanced current copiers that overcome some of those limitations. Then we show how current copiers can be put together in order to build some of the basic building blocks used in many practical applications e.g. sample delays, delay lines, integrators and differentiators. We also discuss some more advanced topics such as nonlinear settling errors and optimization.

The Applications part gives examples of switched current circuits that have been implemented in silicon. This part covers topics such as filters, serial A/D and D/A converters, Sigma-Delta modulators and adaptive filters.

The Appendices part covers topics such as sampling of noise, current transmission errors and switching transients, matching and MOS transconductors. The presentation of these topics is done so they easily fit into the Theory part of this thesis.

The Publications part is an collection of enclosed copies of the papers that I have published during my Ph.D. study.

## Examples

The text in this thesis contains several examples that are used to illustrate some ideas, concepts and circuits. The examples are recognized as sections of text having the following layout.

### Example 0.0.1

This is an example of an example. Please notice that the end of all examples is marked with a small black box. ■

## Acknowledgments

I would like to thank Thomas Kaulberg for a pleasant and enjoyable cooperation on the MAGFET project and for many valuable discussions regarding current mode circuits and techniques.

I would also like to thank Ivan Harald Holger Jørgensen for an enjoyable cooperation on the Adaptive filter project and for doing a tremendous job on the layout of the adaptive

filter. I am also very grateful to Ivan for doing a thorough proof reading the manuscript for this thesis.

I would like to thank Claus Furst, Erik Bruun and Oluf Hogh Olesen for many valuable discussions regarding analog circuits and current mode techniques.

Also I would like to thank OTICON, DANAVOX, MICROTRONIC and DELTA for their interest in my work.

### Typesetting

This thesis has been typeset using L<sup>A</sup>T<sub>E</sub>X 2<sub>ε</sub> in an 11pt Computer Modern Font. All of the figures have been prepared using **CorelDraw** and **Grafer4Windows** and the figures were inserted into the text as Windows-Meta-Files (WMF) using the `\special` command. The bibliography was generated using B<sub>I</sub>B<sub>T</sub>E<sub>X</sub> and the printing of this thesis was performed using the Windows DVI viewer **DviWin**.

*Gudmundur Bogason  
Frederiksberg, September 4, 1995*

# Abstract

## English

This thesis focuses mainly on SI circuits. The treatment of the SI technique is most of the time kept on a high level using transconductors instead of transistor. It is the authors believe that this results in an easier and clearer understanding of the operation of the SI circuits because the circuits are not cluttered with confusing transistors circuits. When needed, transistor circuits are presented in order to show specific implementation details or novel circuitry.

Basic techniques for sampled data system design is presented, and it is shown that linear signal processing functions using nonlinear components in both SI and SC techniques are feasible and that they rely on the same common principles.

The design of current copiers and sampled data building blocks is presented in details, this applies to both single ended and differential circuits. The limitations found in current copiers are discussed and novel new implementations of SI building blocks are presented.

The effect of nonlinear settling errors on the operation of SI circuits is illustrated and it is shown that nonlinear settling errors are caused by the nonlinear transconductors used in the current copier cells. Simulations are presented that show that the effect of the nonlinear settling is an increase in Total-Harmonic-Distortion (THD) with the frequency of the signals. Techniques for reduction of the nonlinear settling errors are outlined and it is shown that highly linear SI circuits require the use of linear transconductors and high bandwidth (large bias current).

Optimization of SI circuits with regards to noise properties is presented and an optimization methodology is outlined that can be used to optimize SI circuits for minimum power consumption for a given Signal-To-Noise-Ratio (SNR). This optimization methodology has further been used in the design of two Sigma-Delta modulators and in the design of an adaptive filter. It is shown that circuits operating in weak inversion are not feasible for the SI technique because of the limited voltage swing found in these circuits.

Practical applications of the SI technique are presented and it is demonstrated that high order filters with good tracking between highpass and lowpass sections, using only MOS transistors and gate-capacitors, are feasible. Also, a serial A/D and D/A conversion system is presented that is capable of offset compensating and converting the current from a MAGFET<sup>1</sup> transistor to a seven bit digital value. This system is implemented in a  $1.5\mu m$  digital CMOS process using only MOS transistors. An adaptive filter with 96 filter taps is implemented in SI technique. The filter is designed to estimate the transfer function of a micromechanical flow channel in order to estimate the flow rate of a fluid flowing in that channel. Also, the design of two Sigma-Delta modulators is presented and a brief discussion of high order modulators is given.

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<sup>1</sup>MOS transistor sensitive to a magnetic field

## Dansk

Denne afhandling omhandler hovedsageligt SI kredsløb. Gennemgangen af SI teknikken er for det meste holdt på et overordnet niveau, ved brug af transkonduktans forstærkere istedet for transistorer. Det er forfatterens overbevisning, at dette vil lette forståelsen for hvordan SI kredsløbene fungerer, fordi kredsløbene ikke bliver forvirrede af uoverskuelige transistor kredsløb. Når det er nødvendigt, anvendes specifikke transistor kredsløb for at illustrere implementerings detaljer og nye kredsløbs koblinger.

Grundlægende teknikker for tidsdiskrete analoge kredsløb er præsenterede og det bliver vist at lineære signal behandlings funktioner v.h.a. ulineære komponenter i både SI og SC teknik er mulige, og at de er baserede på de samme grundlæggende principper.

Design af current copiers og tidsdiskrete byggeblokke bliver præsenteret i detaljer, dette gælder både for almindelige og differentielle kredsløb. De begrænsninger der ligger i current copiers bliver diskuteret og nye implementeringer af SI byggeblokke bliver præsenteret.

Effekten af ikke lineære settling fejl på funktionen af SI kredsløb er illustreret og det bliver vist at ulineære settling fejl skyldes de ulineære transkonduktans forstærkere, der bliver brugt i current copier cellerne. Der bliver præsenteret simuleringer, der viser at effekten af ulineære settling fejl er en stigning af den harmoniske forvrængning (THD) med frekvensen af signalet. Teknikker til reduktion af de ulineære settling fejl bliver skitseret og det bliver vist, at meget lineære SI kredsløb kræver at man bruger lineære transkonduktans forstærkere og høj båndbredde.

Optimering af SI kredsløb m.h.t. støj egenskaber bliver præsenteret, og en optimerings metode bliver skitseret, som kan bruges til at optimere SI kredsløb for et minimalt effekt forbrug for et givet signal støj forhold (SNR). Denne optimerings metode er endvidere blevet brugt til design af to Sigma-Delta modulatorer, og til design af et adaptivt filter. Det bliver vist at kredsløb der fungerer i weak-inversion ikke er velegnede til SI kredsløb p.g.a. det begrænsede spændings sving i disse kredsløb.

Praktiske anvendelser af SI teknikken bliver præsenteret, og det bliver demonstreret at højere ordens filtre med god tracking mellem højpas og lavpas sektionerne er mulige, alene baseret på MOS transistorer og gate-capaciteter. Også et serielt A/D og D/A konverterings system bliver præsenteret, der er i stand til at offset kompensere, og konvertere strømmen fra en MAGFET<sup>2</sup> transistor til et syv bit tal. Systemet er implementeret i en  $1.5\mu\text{m}$  digital CMOS process, alene v.h.a. MOS transistorer. Et adaptivt filter med 96 filter koefficienter er blevet implementeret i SI teknik. Filteret er beregnet til at estimere overførings funktionen af en mikromekanisk flow kanal for at man skal kunne estimere flow hastigheden af en væske i flow kanalen. Der bliver også præsenteret to Sigma-Delta modulatorer, og der bliver givet en kort diskussion af højre ordens modulatorer.

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<sup>2</sup>en MOS transistor der er følsom overfor et magnetisk felt

# Contents

<b>Preface</b>	<b>i</b>
<b>Abstract</b>	<b>iii</b>
<b>Introduction</b>	<b>xx</b>
<b>I Theory</b>	<b>22</b>
<b>1 Basic Techniques for Sampled Data Systems</b>	<b>23</b>
1.1 Switched Capacitor Circuits using Nonlinear Capacitors . . . . .	23
1.1.1 Charge Scaling . . . . .	24
1.1.2 Integrator . . . . .	25
1.2 Switched Current Circuits using Nonlinear Elements . . . . .	26
1.2.1 Current Scaling . . . . .	27
1.2.2 Current Memories . . . . .	27
1.2.3 Sample Delay . . . . .	29
<b>2 Design of Current Copiers</b>	<b>32</b>
2.1 Current Transmission Errors . . . . .	32
2.1.1 Decrease of output conductance and feedback capacitance . . . . .	33
2.1.2 Increase of input conductance . . . . .	34
2.2 Single ended Current Copiers and Current Mirrors . . . . .	34
2.2.1 Simple . . . . .	34
2.2.2 Cascode . . . . .	35
2.2.3 Folded Cascode . . . . .	37
2.2.4 Regulated Cascode . . . . .	37
2.2.5 Regulated Folded Cascode . . . . .	39
2.2.6 Cascode II . . . . .	39
2.3 Differential Current Copiers and Current Mirrors . . . . .	41
2.3.1 Simple . . . . .	42
2.3.2 Cascode and Cascode II . . . . .	42
2.3.3 Fully Differential Current Conveyors and Commonmode Regulation . . . . .	43
<b>3 Design of Switched Current Building Blocks</b>	<b>47</b>
3.1 Sample Delays . . . . .	47
3.2 Delay Lines . . . . .	50
3.2.1 Cascade . . . . .	50
3.2.2 Polyphase . . . . .	50

3.3	Integrators . . . . .	51
3.3.1	Inverting and Non-inverting Integrators . . . . .	51
3.3.2	Bilinear Integrator . . . . .	54
3.4	Differentiators . . . . .	54
<b>4</b>	<b>Settling Errors in Switched Current Circuits</b>	<b>58</b>
4.1	Linear Settling Errors . . . . .	58
4.2	Nonlinear Settling Errors . . . . .	60
4.2.1	Current Copier . . . . .	64
4.2.2	Sample Delays . . . . .	65
4.2.3	Integrators . . . . .	66
4.3	Reduction of Settling errors . . . . .	68
<b>5</b>	<b>Optimization of Switched Current Circuits</b>	<b>73</b>
5.1	Introduction to Noise Analysis . . . . .	73
5.1.1	Signal to Noise Ratio SNR . . . . .	78
5.1.2	Storage Capacitance . . . . .	78
5.1.3	Bias Current . . . . .	79
5.1.4	Power Consumption . . . . .	79
5.1.5	Constraints . . . . .	79
5.2	Optimization . . . . .	80
5.3	Switched Current Circuits Operating in Weak-Inversion . . . . .	85
<b>II</b>	<b>Applications</b>	<b>88</b>
<b>6</b>	<b>Switched Current Micropower 4th Order Lowpass/Highpass - Filter</b>	<b>89</b>
6.1	Design . . . . .	89
6.2	Implementation . . . . .	92
6.2.1	Differentiator . . . . .	94
6.2.2	Sample and Hold . . . . .	95
6.2.3	Current Scaling . . . . .	95
6.2.4	Current Buffer . . . . .	96
6.2.5	Two Phase Clock Generator . . . . .	97
6.3	Layout . . . . .	98
6.4	Experimental Results . . . . .	99
6.4.1	Frequency Response . . . . .	99
6.4.2	Noise Floor . . . . .	101
6.5	Conclusion and Future Work . . . . .	101
<b>7</b>	<b>Switched Current Adaptive Filter for Estimating Flow rates in Micromechanical Flow Channels</b>	<b>106</b>
7.1	Flow Estimation . . . . .	106
7.2	Adaptive Filter . . . . .	107
7.2.1	Simulation of the Adaptive Filter . . . . .	110
7.3	Implementation . . . . .	111
7.3.1	Input Sections . . . . .	112
7.3.2	Filter Tap . . . . .	114
7.3.3	Delay line and FSM . . . . .	115
7.4	Layout . . . . .	116

7.5	Experimental Results . . . . .	116
7.6	Conclusion and Future Work . . . . .	118
<b>8</b>	<b>Serial A/D and D/A Converter</b>	<b>119</b>
8.1	Introduction . . . . .	119
8.1.1	The “Digital” solution . . . . .	120
8.1.2	The Analog solution . . . . .	120
8.2	The SI A/D – D/A System . . . . .	121
8.2.1	Introduction . . . . .	122
8.2.2	Operation of the A/D – D/A system . . . . .	123
8.2.3	Analog building blocks . . . . .	126
8.2.4	Digital Building Blocks . . . . .	129
8.2.5	Error Analysis . . . . .	130
8.3	Layout . . . . .	132
8.4	Experimental Results . . . . .	132
8.5	Conclusion and Future Work . . . . .	134
<b>9</b>	<b>Switched Current Micropower 2nd Order Sigma-Delta A/D Converter</b>	<b>135</b>
9.1	Design . . . . .	135
9.2	Implementation . . . . .	137
9.2.1	DAC’s . . . . .	138
9.2.2	Integrators . . . . .	139
9.2.3	Comparator . . . . .	143
9.3	Experimental Results . . . . .	143
9.4	Conclusion and Future Work . . . . .	143
<b>10</b>	<b>Switched Current 3rd Order Sigma-Delta A/D Converter</b>	<b>145</b>
10.1	Why use high-order modulators . . . . .	145
10.2	Stability problems . . . . .	145
10.3	Modulator topology . . . . .	146
10.4	Modulator filter and stability analysis . . . . .	148
10.5	Design of Modulator filter . . . . .	149
10.5.1	Simulation of the Modulator . . . . .	151
10.6	Implementation . . . . .	153
10.6.1	Input section and Feed-Input . . . . .	155
10.6.2	Integrators and Feedback DAC’s . . . . .	155
10.6.3	Comparator . . . . .	157
10.7	Layout . . . . .	158
10.8	Experimental Results . . . . .	158
10.9	Conclusion and Future Work . . . . .	159
<b>11</b>	<b>Conclusions</b>	<b>160</b>
<b>III</b>	<b>Appendix</b>	<b>167</b>
<b>A</b>	<b>MOS Transconductors</b>	<b>168</b>
A.1	The MOS Transistor . . . . .	168
A.2	The Compound MOS Transistor . . . . .	169
A.3	The MOS Differential pair . . . . .	170



A.3.1	Relationship between output current and differential voltage . . . . .	170
A.3.2	Relationship between transconductance and differential voltage . . . . .	172
A.3.3	Relationship between source voltage $v_S$ and the voltages $v_1$ and $v_2$ . . . . .	172
A.4	Resistor Degenerated Differential pair . . . . .	173
A.5	Linear MOS Transconductors . . . . .	175
A.5.1	Linearized MOS Differential pair . . . . .	176
<b>B</b>	<b>Current Transmission Errors</b>	<b>178</b>
<b>C</b>	<b>Switching Transients</b>	<b>180</b>
<b>D</b>	<b>Clock Feedthrough and Charge Injection</b>	<b>184</b>
D.1	Modeling the MOS switch . . . . .	184
D.2	Switched Capacitor . . . . .	187
D.3	Current Copier . . . . .	189
D.3.1	Linear effects . . . . .	190
D.4	Integrator . . . . .	190
<b>E</b>	<b>Noise in Sampled Data Systems</b>	<b>192</b>
E.1	Introduction . . . . .	192
E.2	Sampling of Noise . . . . .	194
E.3	Sampling of White Noise . . . . .	195
E.4	Sampling of $1/f$ Noise . . . . .	197
E.5	Noise power at the output of a large system . . . . .	198
E.6	Correlated Double Sampling (CDS) of $1/f$ Noise . . . . .	199
<b>F</b>	<b>Matching Errors</b>	<b>200</b>
F.1	Introduction . . . . .	200
F.2	Single MOS transistor . . . . .	202
F.3	Parallel connection of unity transistors . . . . .	204
F.4	Current mirror using unity transistors . . . . .	204
<b>IV</b>	<b>Publications</b>	<b>206</b>

# List of Figures

1.1	Linear charge mirror utilizing nonlinear capacitors . . . . .	24
1.2	Relationship between input charge packets and output charge. Simulation performed using PSPICE . . . . .	25
1.3	Cascade of two parasitic insensitive SC integrators utilizing nonlinear capacitors.	26
1.4	Current Mirror used for amplification or scaling of signal currents and the corresponding signal flow graph (SFG). . . . .	27
1.5	1st generation current memory and the corresponding signal flow graph (SFG).	28
1.6	2nd generation current memory (Current Copier) and the corresponding signal flow graph (SFG). . . . .	28
1.7	Timing of the clock phases used in the current memories . . . . .	29
1.8	Sample delay using cascading of two current copiers and its corresponding SFG.	30
1.9	Implementation of a sample delay using single MOS transistors as transconductors. . . . .	30
1.10	Simulation of the implemented sample delay for a single input current pulse .	31
2.1	Basic current copier including its parasitics . . . . .	32
2.2	Cascode . . . . .	33
2.3	Regulated cascode . . . . .	33
2.4	Cascode II . . . . .	34
2.5	Simple Current Copier . . . . .	35
2.6	Cascode Current Copier . . . . .	36
2.7	Folded Cascode Current Copier . . . . .	37
2.8	Regulated Cascode Current Conveyor . . . . .	38
2.9	Regulated Folded Cascode Current Copier . . . . .	39
2.10	Cascode II Current Copier . . . . .	40
2.11	Class AB, Cascode II Current Copier . . . . .	41
2.12	Simple Fully Differential Current Copier . . . . .	42
2.13	Fully Differential Cascode Current Copier . . . . .	43
2.14	Fully Differential Cascode II Current Copier . . . . .	44
2.15	Fully differential CCII– including a commonmode regulation based on resistor degeneration . . . . .	45
2.16	Fully differential CCII– including a commonmode regulation based on current steering . . . . .	45
2.17	Fully differential CCII– including a commonmode regulation based on current steering . . . . .	46
3.1	Sample Delay made from cascading of two current copiers . . . . .	48
3.2	Sample Delay made from cascading of two Cascode II current copiers . . . . .	48
3.3	(a) Simplified Delay made from cascading of two Cascode II CCOP’s; (b) Final Sample Delay made from cascading of Cascode II CCOP’s . . . . .	49

3.4	(a) Cascode implementation of sample delay; (b) Folded Cascode implementation of sample delay . . . . .	49
3.5	Delay Line made from cascoding of sample delays . . . . .	50
3.6	Polyphase delay line . . . . .	51
3.7	(a) Inverting and Noninverting Integrator; (b) Simplified Integrator . . . . .	52
3.8	SFG for the Inverting and Noninverting Integrator . . . . .	52
3.9	(a) Inverting and Noninverting integrator based on Cascode II current copiers; (b) Simplified Inverting and Noninverting integrator based on Cascode II current copiers . . . . .	53
3.10	(a) Cascode implementation of the integrator; (b) Folded Cascode implementation of the integrator . . . . .	53
3.11	Fully differential bilinear integrator . . . . .	54
3.12	(a) Core component in all switched current differentiators; (b) Simplified Core component used in all switched current differentiators . . . . .	55
3.13	(a) Differentiator followed by a Track and Hold; (b) Track and Hold followed by a Differentiator . . . . .	56
3.14	(a) Differentiator based on the Cascode II current copier; (b) Simplified differentiator . . . . .	56
3.15	(a) Cascode implementation of differentiator; (b) Folded Cascode implementation of differentiator . . . . .	57
4.1	A current copier without its parasitics. . . . .	58
4.2	Voltage sequence at the storage capacitor in the linear current copier, for a single current pulse at the input. . . . .	59
4.3	SFG describing the effect of linear settling error in a current copier. . . . .	60
4.4	Nonlinear transconductor used in the current copier . . . . .	61
4.5	Block diagram showing the generation of the distorted output current in a nonlinear current copier . . . . .	62
4.6	Simplified block diagram showing the generation of the distorted output current in a nonlinear current copier . . . . .	62
4.7	Current copier used for distortion simulations . . . . .	63
4.8	Frequency spectrum at the output of the current copier . . . . .	64
4.9	Distortion (THD) as a function of input frequency for the current copier . . . . .	65
4.10	Frequency spectrum at the output of the sample delay . . . . .	66
4.11	Frequency spectrum at the output of the double sample delay . . . . .	67
4.12	Distortion (THD) as a function of input frequency for the current copier and the sample delays . . . . .	68
4.13	Frequency spectrum of the inverting output of the integrator . . . . .	69
4.14	Frequency spectrum of the noninverting output of the integrator . . . . .	70
4.15	Distortion (THD) as a function of the input frequency for the integrator . . . . .	70
4.16	Frequency spectrum at the inverting output of the integrator (Differential Transconductor) . . . . .	71
4.17	Frequency spectrum at the noninverting output of the integrator (Differential Transconductor) . . . . .	71
4.18	Distortion (THD) as a function of input frequency for the integrator (Differential Transconductor) . . . . .	72
5.1	Cascode Current Copier with all Noise Sources . . . . .	73
5.2	Noise from a Cascoded MOS Transistor . . . . .	75

5.3	Cascode Current Copier shown with its equivalent input noise source . . . . .	75
5.4	SFG representing the noise sampling . . . . .	76
5.5	Sample delay made from cascading two Cascode Current Copiers . . . . .	81
5.6	Cascade of Folded Cascode Current Copiers . . . . .	82
5.7	Minimized Capacitance dependence on Supply Voltage. The capacitance is normalized with: $\text{SNR} \cdot \frac{48}{3}kT$ . . . . .	83
5.8	Power Consumption for Minimized Capacitance. The power consumption is normalized with: $\omega_0 \cdot \text{SNR} \cdot \frac{48}{3}kT$ . . . . .	84
5.9	Minimized Power Consumption dependence on Supply Voltage. The power consumption is normalized with: $\omega_0 \cdot \text{SNR} \cdot \frac{48}{3}kT$ . . . . .	84
5.10	Capacitance for Minimized Power Consumption. The capacitance is normalized with: $\text{SNR} \cdot \frac{48}{3}kT$ . . . . .	85
5.11	Minimized Bias Current dependence on Supply Voltage. The bias current is normalized with: $\omega_0 \cdot \text{SNR} \cdot \frac{48}{3}kT$ . . . . .	86
6.1	Biquad filters section, using sample delays . . . . .	89
6.2	SFG for lowpass and highpass filters . . . . .	91
6.3	Transposed SFG for lowpass and highpass filters. . . . .	92
6.4	Filter Structure based on the transposed SFG . . . . .	92
6.5	Transconductor used in all of the building blocks in the filter . . . . .	93
6.6	Diagram of the differentiator . . . . .	95
6.7	Sample and Hold (S/H) . . . . .	96
6.8	Diagram of the current amplifier A2 . . . . .	96
6.9	Diagram of the Input and Output Buffer . . . . .	97
6.10	Diagram of the Two phase Clock generator . . . . .	97
6.11	Layout of the filter chip . . . . .	98
6.12	Layout of a differentiator . . . . .	99
6.13	Layout of the current amplifier A2 . . . . .	100
6.14	Frequency response with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 2.0V$ . . . . .	101
6.15	Frequency response with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 3.3V$ . . . . .	102
6.16	Frequency response with a sampling frequency of $f_s = 50kHz$ and at a supply voltage of $V_{DD} = 2.0V$ . . . . .	103
6.17	Frequency response with a sampling frequency of $f_s = 50kHz$ and at a supply voltage of $V_{DD} = 3.3V$ . . . . .	103
6.18	Lowpass output noise with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 2.0V$ . . . . .	104
6.19	Lowpass output noise with a sampling frequency of $f_s = 50kHz$ and at a supply voltage of $V_{DD} = 2.0V$ . . . . .	104
6.20	Highpass output noise with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 3.3V$ . . . . .	105
7.1	Impulse response of the flow channel . . . . .	107
7.2	FIR filter used for estimating the impulse response . . . . .	107
7.3	Flow channel including Adaptive filter for flow estimation . . . . .	108
7.4	Adaptive filter incorporating the LMS algorithm . . . . .	109
7.5	Time history of the numerically largest filter tap, estimating the delay in the flow channel (Flow rate) . . . . .	110

7.6	Filter taps after 4096 iterations of the adaptive filter . . . . .	111
7.7	Filter tap No. 25 as a function of time . . . . .	112
7.8	Sample/Hold and Differentiator . . . . .	113
7.9	Comparator . . . . .	113
7.10	1-Bit DAC . . . . .	114
7.11	The $i$ th filter tap . . . . .	115
7.12	Delay line and FSM . . . . .	115
7.13	Layout of the Adaptive Filter . . . . .	116
7.14	Layout of a single filter tap . . . . .	117
8.1	Basic configuration of the Angledetecting system . . . . .	119
8.2	Approximate <i>Angle to Magnetic flux</i> transfer function . . . . .	120
8.3	‘Two MAGFET’ implementation . . . . .	121
8.4	The MAGFET signal currents . . . . .	121
8.5	Block diagram of the A/D – D/A system . . . . .	124
8.6	Diagram of the transconductor used in the current copier cells . . . . .	127
8.7	MAGFET interface . . . . .	127
8.8	Block diagram of the staircase generator . . . . .	128
8.9	Block diagram of the accumulator . . . . .	129
8.10	Block diagram of the current comparator . . . . .	129
8.11	Two phase non-overlapping Clock generator . . . . .	130
8.12	Linearity of D/A around MSB, with $c = 0.49$ . . . . .	131
8.13	Linearity of D/A around MSB, with $c = 0.52$ . . . . .	132
8.14	Layout of the core of the MAGFET chip . . . . .	133
9.1	Basic Sigma-Delta Modulator . . . . .	136
9.2	Amplitude distribution of internal signal swing in the integrators for the basic sigma-delta modulator . . . . .	136
9.3	Modified Sigma-Delta Modulator, for reduced internal signal swing . . . . .	136
9.4	Amplitude distribution of internal signal swing in the integrators for the mod- ified sigma-delta modulator . . . . .	137
9.5	SNR for different input amplitudes at the input of the modulator . . . . .	138
9.6	Block diagram of the fully differential 2nd order sigma-delta modulator . . . . .	138
9.7	1-Bit DAC . . . . .	139
9.8	Integrator INT1 and DAC1 . . . . .	139
9.9	Integrator INT2 . . . . .	142
9.10	Fully differential regenerative voltage Comparator . . . . .	143
10.1	Modulator topology . . . . .	147
10.2	Generic Modulator with linearized quantizer . . . . .	147
10.3	Noise-shaping modulator structure . . . . .	147
10.4	Estimated Signal Transfer Function $STF_{K_n}(z)$ . . . . .	150
10.5	Plot of maximum transient length versus constant input . . . . .	151
10.6	Amplitude distribution at the output of the integrators for an input signal of 0.43 and without multiple feed-input . . . . .	152
10.7	Amplitude distribution at the output of the integrators for an input signal of 0.43 and with multiple feed-input . . . . .	153
10.8	Modulator output spectrum with a relative input amplitude of 0.45 (MSA), without settling errors and with settling errors of 0.5% . . . . .	154
10.9	Block diagram of the Sigma-Delta Modulator . . . . .	155

10.10	Block diagram of the Input section and Feed-Input . . . . .	156
10.11	Block diagram of the 1st and the 2nd integrator . . . . .	156
10.12	Block diagram of the 3rd integrator . . . . .	157
10.13	Block diagram of the comparator . . . . .	157
10.14	Layout of the 3rd order Sigma-Delta Modulator . . . . .	158
A.1	A single MOS transistor . . . . .	168
A.2	A compound MOS transistor . . . . .	169
A.3	MOS Differential pair . . . . .	170
A.4	Relationship between differential output current and differential input voltage for a MOS differential pair . . . . .	172
A.5	Relationship between transconductance and differential input voltage for a MOS differential pair . . . . .	173
A.6	Plot of the function $f(x)$ . . . . .	174
A.7	A MOS differential pair degenerated with two resistors . . . . .	174
A.8	MOS transistors used in a linear transconductor . . . . .	175
A.9	Plot of the output currents of the linear MOS transconductor . . . . .	177
B.1	A current output feeding the input of a current mirror. . . . .	178
B.2	A current copier in hold mode feeding the input of an other current copier in the copy phase. . . . .	179
C.1	A current copier in its copy phase. . . . .	180
C.2	A current copier in its hold phase while feeding the input of an other current copier. . . . .	182
C.3	Settling response given by (C.9) . . . . .	182
D.1	NMOS transistor used as switch . . . . .	184
D.2	A distributed RC model for the NMOS transistor . . . . .	184
D.3	A small section of the distributed RC model of the NMOS transistor . . . . .	185
D.4	Voltage at the gate of the switch . . . . .	186
D.5	Lumped Model of a NMOS switch; (a) switch is in its on state; (b) switch is off	187
D.6	Voltage signal source, feeding a switched capacitor . . . . .	187
D.7	Switched capacitor with a lumped model for the switch . . . . .	187
D.8	Switch induced error voltage for different switching ratios . . . . .	189
D.9	A current copier showing the switch that causes errors . . . . .	190
D.10	SFG showing the effect of clock feedthrough and charge injection in SI integrators. . . . .	191
E.1	Capacitor shunted by a noisy resistor . . . . .	192
E.2	Illustration of the undersampling of bandlimited white noise: (a) bandwidth equal to sampling frequency; (b) bandwidth equal to twice sampling frequency	195
E.3	Sum of the replica of the squared magnitude of the transfer function for a 1st order lowpass filter . . . . .	197
E.4	Shape of the power spectrum for a sampled $1/f$ noise source . . . . .	198
F.1	A Current Copier with an extra current output . . . . .	200
F.2	A simple implementation of a Current Copier; with a extra current output; in its copy phase i.e. phase 1 . . . . .	201
F.3	Parallel connection of $N$ unity transistors . . . . .	204

F.4 Current mirror made from unity transistors . . . . . 205

# List of Tables

1.1	Parameters used in the simulation of the implemented sample delay . . . . .	31
4.1	Parameters used for the current copier . . . . .	63
6.1	Typical Process parameters for the $2.4\mu m$ CMOS process (MIETEC) . . . . .	93
6.2	Saturation voltages and the peak signal current used in the transconductor . . . . .	94
7.1	Parameters used for the simulation of the flow channel . . . . .	110
9.1	Saturation voltages and storage capacitance found for the Sigma-Delta modulator . . . . .	142
10.1	Modulator Coefficients scaled for minimum signal swing without feed-input . . . . .	149
10.2	Modulator Coefficients scaled for minimum signal swing with feed-input . . . . .	150
10.3	Relationship between small signal settling error $\epsilon$ and resulting SNR . . . . .	153
10.4	Data for one of the transconductors used in the first integrator, for different choices of $V_{DD}$ . Parameters in the optimization:Relative input amplitude = 0.5, Settling error = 0.5%, Modulation Index $m_i = 0.77$ . . . . .	154
10.5	Saturation voltages used in the SI circuits i.e. Integrators and Biasing circuitry	155
D.1	Parameters used for the switched capacitor circuit . . . . .	188
E.1	Noise Bandwidth BWN, for lowpass filters of order n. . . . .	196



# List of Abbreviations

SI	Switched - Current.
SC	Switched - Capacitor.
CCII-	Second generation Current Conveyor, minus type.
CCII+	Second generation Current Conveyor, plus type.
OTA	Operational Transconductance Amplifier.
VOA	Voltage Mode Operational Amplifier.
COA	Current Mode Operational Amplifier.
CFB	Current Feedback Amplifier.
CCOP	Current Copier.
CM	Current Mirror.
MOS	Metal Oxide Semiconductor.
A/D	Analog to Digital.
D/A	Digital to Analog.
MSB	Most Significant Bit.
LSB	Least Significant Bit.
MASH	Multistage Noise Shaping.
SDM	Sigma-Delta Modulator.
$\Sigma\Delta$	Sigma-Delta.
SFG	Signal Flow Graph.
VLSI	Very Large Scale Integration.
CMR	Comonmode Regulation.
CMRR	Comonmode Rejection Ratio.
PSRR	Power Supply Rejection Ratio.
MPW	Multi Project Wafer.
FSM	Finite State Machine.

# List of Notations

## Physical paramers

Oxide thicknes.

$$t_{OX}$$

Oxide capacitance per area.

$$C'_{OX} = \frac{\epsilon_{Si}}{t_{OX}}$$

mobility.

$$\mu$$

Transconductance parameter.

$$K' = \mu C'_{OX}$$

## MOS transistor paramers

Channel width.

$$W$$

Channel length.

$$L$$

Transconductance parameter.

$$\beta = \frac{W}{L} K'$$

Threshhold Voltage.

$$V_T$$

Gate-Source Voltage

$$v_{GS}$$

Drain-Source Voltage

$$v_{DS}$$

Saturation voltage.

$$\Delta v = V_{GS} - V_T$$

**Signal analysis**

Sequence.

$$x[n]$$

Finite length sequence.

$$x[n], 0 \leq n \leq N - 1$$

Matrix and Vector.

$$\mathbf{x}$$

Transposed.

$$\mathbf{x}^T$$

Conjugate.

$$\mathbf{x}^*$$

Finite length sequence as vector.

$$\mathbf{x} = \begin{bmatrix} x[0] \\ x[1] \\ \vdots \\ x[N - 1] \end{bmatrix}$$

Analog autocorrelation.

$$R_x(\tau)$$

Analog power spectral density.

$$S_x(f)$$

Sampled analog autocorrelation.

$$r_x(\tau)$$

Sampled analog power spectral density.

$$s_x(f)$$

Digital autocorrelation.

$$r_x[m]$$

Digital power spectrum.

$$s_x(e^{j2\pi f \Delta T})$$

Fourier pair.

$$g(t) \leftrightarrow G(f)$$

Analog Fourier transform.

$$G(f) = \int_{-\infty}^{+\infty} g(t) e^{-j2\pi ft} dt$$

Inverse Analog Fourier transform.

$$g(t) = \int_{-\infty}^{+\infty} G(f) e^{j2\pi ft} df$$

Analog Convolution.

$$g_1(t) \otimes g_2(t) = \int_{-\infty}^{+\infty} g_1(\theta) g_2(t - \theta) d\theta$$

$$g_1(t)g_2(t) \leftrightarrow G_1(f) \otimes G_2(f)$$

$$g_1(t) \otimes g_2(t) \leftrightarrow G_1(f)G_2(f)$$

Digital Fourier transform.

$$G(f) = \sum_{n=-\infty}^{+\infty} g[n]e^{-j2\pi fn\Delta T}$$

Inverse Digital Fourier transform.

$$g[n] = \frac{1}{f_s} \int_{-f_s/2}^{+f_s/2} G(f)e^{j2\pi fn\Delta T} df$$

Discrete Fourier Transform.

$$G[m] = \frac{1}{N} \sum_{n=0}^{N-1} g[n]e^{-jmn\frac{2\pi}{N}}$$

Inverse Discrete Fourier Transform.

$$g[n] = \sum_{m=0}^{N-1} G[m]e^{jmn\frac{2\pi}{N}}$$

# Introduction

The development of integrated circuit processing technology has now reach a stage where it is possible to integrate several millions transistors on a single chip. Chip's containing approximately 10 million transistors have been reported.

Processing technology is being tuned for optimum performance for digital circuits. This implies shrinking device sizes for increasing speed and lowering the supply voltage for reduced power consumption.

It is mainly digital circuits that have gained most from the evolving processing technology. It is therefore natural to se more and more signalprocessing function performed digitally.

Large analog chip's are rare now at days. The analog circuitry is now mostly used for interfacing the digital circuits to the outside world. The main functions for analog circuits, in mixed mode designs, are therefore data conversion and filtering.

Traditionally switched capacitor (SC) circuits have been used extensively in the analog interface portion of mixed mode integrated circuits. They have been used for filtering , A/D and D/A conversion and many other interfacing functions.

Switched current (SI) circuits have recently been proposed as a possible replacement or an alternative to SC circuits in mixed mode designs. The motivation for this has been that processing technology is being tuned for digital designs implying that there might be no good analog components left such as: large double poly capacitors etc. which normally are required in SC circuits.

Also, it has often been said that SI circuits can be designed using modest circuitry, i.e. only MOS transistors and nonlinear capacitors e.g. gate-source capacitors, which of course make SI circuits perfect for digital CMOS processes.

In this thesis I will show that the above statements are only true with some slight modifications. It will be shown that linear SC circuits can be designed using nonlinear capacitors, making SC circuits compatible with digital CMOS processes and that high performance SI circuits do require the same circuit complexity as SC circuits.

The main objective of this thesis is to investigate techniques for design of SI circuits with performance comparable to SC circuits. This implies that we look at different current copier cells and how to enhance them, it also implies that we look at noise in SI circuits and how to design for low power and low noise. Also, because SI circuits are inherently nonlinear we look at how nonlinear settling affects the operation of SI circuits.

Switched capacitor circuits can in most cases be analyzed as being linear circuits and there exists a lot of different design and analysis tools for SC circuits. There is however one crucial difference between SC and SI circuits. SI circuits are inherently nonlinear. Because of this difference it is necessary to use different design tools to make full use of the SI technique. Some efforts have been made to designing tools for SI circuits, but all of these tools assume that SI circuits are linear. Until now the only tool available for simulating nonlinearities in SI circuits has been SPICE.

As long as small circuits are being analyzed, such as current copiers etc., it is possible to use SPICE, but for moderately large SI circuits such as Sigma-Delta Modulators it is not feasible to use SPICE for simulating the effect of nonlinearities in the SI circuits because of the excessively long simulation time.

Because of these limitations, I have in this thesis combined several tools, in order to cope with the complexity and simulation requirements of the SI circuits. Some of these tools are: PSPICE, which is used for detailed circuit level simulation, although it sometimes results in excessive simulation times. C++, which is used for behavioral level simulations, making it possible to simulate the effect of nonlinear settling errors on large SI circuits. MATLAB, which is used for optimization of SI circuits and for post processing of simulation results.

**Part I**  
**Theory**

# Chapter 1

## Basic Techniques for Sampled Data Systems

The aim of this chapter is to introduce the most basic building blocks used in most analog sampled data systems today i.e. switched–capacitor [1][2][3] and switched–current circuits. The main point in this introduction will be to show that both SC and SI circuits are compatible with digital CMOS processes (single Poly processes), i.e. CMOS processes that do not support large linear floating capacitors, and that linear analog sampled data systems can easily be built using nonlinear capacitors (voltage dependent) in the SC case and using nonlinear transconductors and capacitors in the SI case.

This chapter also introduces signal flow graphs (SFG) as an powerful tool for analyzing and synthesizing SI circuits. It is assumed that the reader is familiar with the notation of  $z$ -transforms as it is the fundamental tool for describing sampled data systems just as laplace-transform is used for describing continuous-time circuits.

### 1.1 Switched Capacitor Circuits using Nonlinear Capacitors

It is well known that linear scaling of signal currents is possible using current mirrors, that are based on transconductors with a nonlinear relationship between the input voltage and the output current (MOS transistors). In a similar way it is also possible to design switched capacitor (SC) circuits performing linear signal processing using nonlinear capacitors. This can be done by using charge mirrors [4].

The consequence of this fact is that linear SC filters can be implemented without the need for double Poly processes i.e. they can be implemented in digital CMOS processes.

In order to illustrate the operation of the charge mirror, we will assume that the capacitors that are voltage dependent have the following relationship between capacitance and voltage.

$$C = C(v) = C_0(1 + c_1v + c_2v^2) \tag{1.1}$$

here  $C_0$  is the zero voltage capacitance and  $v$  is the applied voltage on the capacitor. The coefficients  $c_1$  and  $c_2$  represents the degree of nonlinearity. This type of voltage dependence is implemented in SPICE exactly as shown in the above equation. When a capacitor has a voltage dependence as shown in the above equation, the orientation of the capacitor becomes important if the voltage dependence contains odd order terms such as  $c_1$ .

The current through the capacitor is found as the derivative of the voltage times the



capacitance

$$i = C \frac{dv}{dt} = C_0(1 + c_1v + c_2v^2) \frac{dv}{dt} = C_0 \left( \frac{dv}{dt} + \frac{1}{2}c_1 \frac{d(v^2)}{dt} + \frac{1}{3}c_2 \frac{d(v^3)}{dt} \right) \quad (1.2)$$

The charge on the nonlinear capacitor can be found by integrating the current through the capacitance

$$q = \int i \, dt = C_0 \left( v + \frac{1}{2}c_1v^2 + \frac{1}{3}c_2v^3 \right) = C_0f(v) \quad (1.3)$$

From this equation we see that the charge on a nonlinear capacitor can in general terms be represented as some zero voltage capacitance  $C_0$  multiplied by a nonlinear function  $f(v)$  of the applied voltage.

### 1.1.1 Charge Scaling

If we want to perform linear signal processing of charges we can do that utilizing charge mirrors. A charge mirror capable of performing linear charge scaling, using nonlinear capacitors, is shown in Fig. 1.1. Please note that the orientation of the nonlinear capacitor is explicitly shown with the plus (+) and minus (-) signs. The operation of the charge mirror shown in

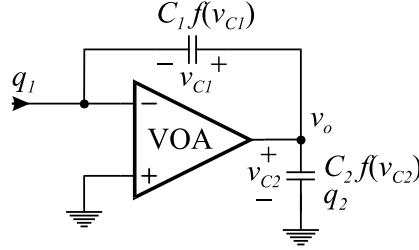


Figure 1.1: Linear charge mirror utilizing nonlinear capacitors

Fig. 1.1 can be described in the following way: The input charge  $q_1$  enters the inverting input of the operational amplifier and is put on the capacitor  $C_1$  this gives the following voltage across the capacitor  $C_1$

$$-q_1 = C_1f(v_{C_1}) \Leftrightarrow v_{C_1} = f^{-1}\left(\frac{-q_1}{C_1}\right) \quad (1.4)$$

Assuming that the operational amplifier is ideal, i.e. the voltage at the negative input (-) is zero (Virtual Ground), the voltage at the output of the operational amplifier is given by

$$v_0 = v_{C_1} = f^{-1}\left(\frac{-q_1}{C_1}\right) \quad (1.5)$$

this voltage is applied to the capacitor  $C_2$ , which gives a charge of

$$q_2 = C_2f(v_0) = C_2f\left(f^{-1}\left(\frac{-q_1}{C_1}\right)\right) \quad (1.6)$$

the function of the inverse function,  $f(f^{-1}(\cdot)) = (\cdot)$ , cancels out and we end up with the following relationship for the charge transfer

$$q_2 = -q_1 \frac{C_2}{C_1} \quad (1.7)$$

This shows that the circuit will act as an inverting linear charge mirror, with a mirroring factor determined by the ratio between the zero voltage capacitors. The constraint for getting linear charge transfer is that the two capacitors  $C_1$  and  $C_2$  must have the same voltage dependence  $f(\cdot)$ , and that they are orientated in a way so that their nonlinearities are adjacent as shown in Fig. 1.1.

### Example 1.1.1

This example illustrates that it is possible to get a linear relationship between input charge and output charge using nonlinear capacitors. This example is based on the configuration shown in Fig. 1.1. The capacitors  $C_1$  and  $C_2$  have both the following nonlinearities:  $c_1 = 2$  and  $c_2 = 3$ . Also the zero voltage capacitors are  $C_1 = 10pF$  and  $C_2 = 20pF$ . The input

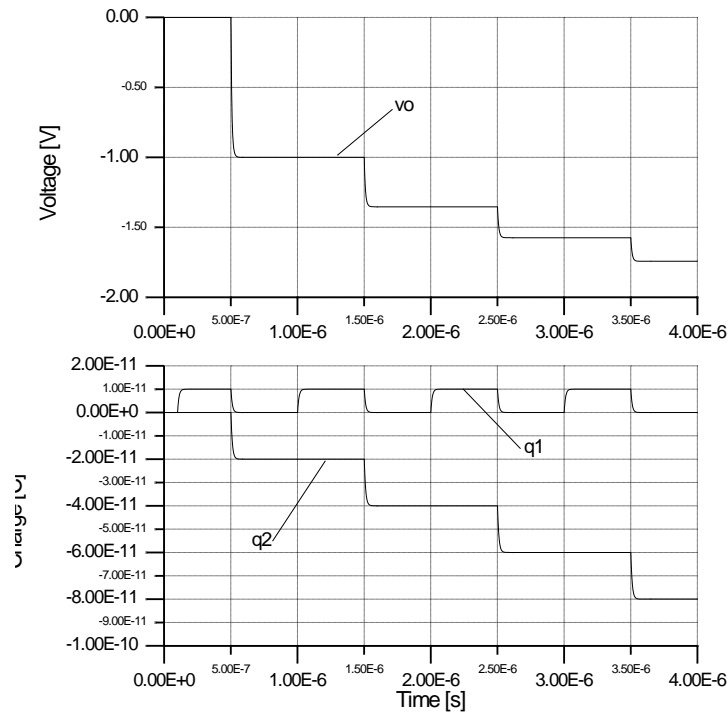


Figure 1.2: Relationship between input charge packets and output charge. Simulation performed using PSPICE

to the charge mirror is a periodic sequence of charge packages  $q_1$  each carrying a charge of  $10pC$ . The charge packages are accumulated on the capacitor  $C_1$ , and this gives the output voltage  $v_o$  shown in Fig. 1.2. We notice that there is a nonlinear relationship between the output voltage  $v_o$  and the charge  $q_1$ .

Also in Fig. 1.2 we see the charge  $q_2$  put on the capacitor  $C_2$ . We notice that for each charge package  $q_1$  of  $10pC$  entering the charge mirror, the charge on capacitor  $C_2$  is decremented by  $20pC$ . This indicates that the circuit operates as an inverting charge mirror with a scaling factor of  $C_2/C_1 = 20pF/10pF = 2$ , as expected. ■

### 1.1.2 Integrator

Most switched capacitor circuits rely on the use of integrators. It is therefore of great interest to be able to design switched capacitor integrators using nonlinear capacitors. The circuit

in Fig. 1.3 shows how it is possible to perform linear signal processing utilizing non-linear capacitors. In Fig. 1.3 there are two linear capacitors  $C_1, C_4$  and two nonlinear capacitors

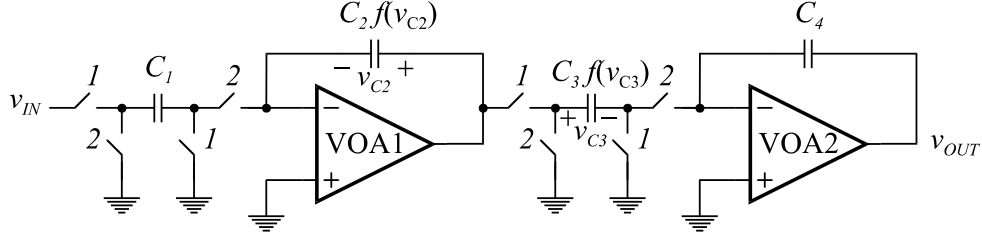


Figure 1.3: Cascade of two parasitic insensitive SC integrators utilizing nonlinear capacitors.

$C_2, C_3$ . The linear capacitor  $C_1$  is used to convert the input voltage  $v_{IN}$  to a linear charge  $q_1$  on clock phase 1. This charge is then on clock phase 2 put on the nonlinear capacitor  $C_2$ . On clock phase 1 the nonlinear voltage at the output of operation amplifier VOA1 is placed on the nonlinear capacitor  $C_3$ , which then gets a charge corresponding to

$$q_2 = -q_1 \frac{C_2}{C_1} \quad (1.8)$$

as shown in the previous subsection on Charge Mirrors.

The first operational amplifier VOA1 together with the nonlinear capacitors  $C_2$  and  $C_3$  acts as a linear charge mirror. On clock phase 2 the linear charge on the nonlinear capacitor  $C_3$  is put on the linear capacitor  $C_4$ , which in turn gives a linear output voltage at the output of operational amplifier VOA2.

## 1.2 Switched Current Circuits using Nonlinear Elements

The basic building blocks necessary for design of SI circuits are a switch, a grounded capacitor and an inverting transconductor. The capacitor and the transconductor do not have to be linear, although it will be shown later in Chapter 4, that in order to design SI circuits with low distortion it is necessary to consider the nonlinearities in the SI circuit elements.

The switch used in a SI circuit can be a NMOS, PMOS or CMOS switch depending on the actual implementation and on the use of the switch. The capacitor can be the gate-source capacitance  $C_{GS}$  of a MOS transistor or it can be some other capacitor probably a MOS transistor coupled as a MOS capacitor. The transconductor can be build using a variety of configuration depending upon the application of the SI circuit. It can be a simple single transistor transconductor (Most often used for illustration) or it can be more complex using variety of cascoding arrangements for enhancing the performance. It can also be both single ended or fully differential and operating in class A or class AB. Different implementations of SI circuits will be described in Chapter 2 and Chapter 3.

The operation of SI circuits is based on the conversion of a signal current to a corresponding signal voltage, using a transconductor. The signal voltage can then be stored on a capacitor for later use, where it then is converted back to a signal current using a transconductor. The transconductors used for converting the signal current to a voltage and then back to a signal current again needs not be the same.

### 1.2.1 Current Scaling

All signal processing operations rely on the possibility of amplification or signal scaling of some sort. In switched current circuits we want to be able to amplify and scale signal currents. This operation is basically done using current mirrors. In Fig. 1.4 OTA0 is used

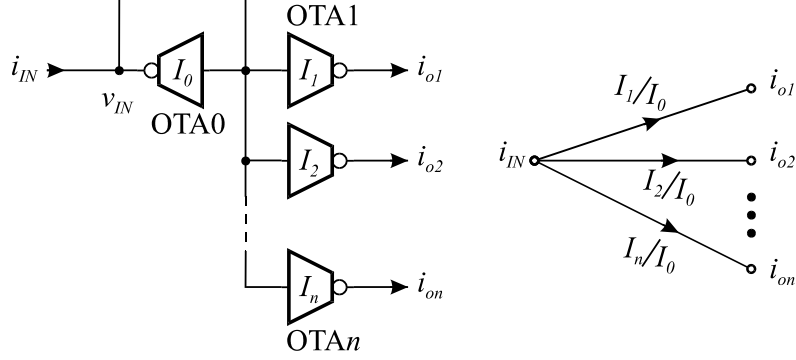


Figure 1.4: Current Mirror used for amplification or scaling of signal currents and the corresponding signal flow graph (SFG).

for converting the input current  $i_{IN}$  to a voltage  $v_{IN}$  that is applied to the inputs of the transconductors OTA1 to OTAn. Each transconductor contains a current  $I_n$  that represents the scaling factor of nonlinear transconductor. We have that:

$$i_{IN} = I_0 f(v_{IN}) \Leftrightarrow v_{IN} = f^{-1}\left(\frac{i_{IN}}{I_0}\right) \quad (1.9)$$

and the output current from transconductor  $i$  is given by:

$$i_{oi} = -I_i f(v_{IN}) = -I_i f\left(f^{-1}\left(\frac{i_{IN}}{I_0}\right)\right) = -i_{IN} \frac{I_i}{I_0} \quad (1.10)$$

So the current at output  $i$  will have a scaling factor of  $-I_i/I_0$ . We observe that in order to get a linear current scaling any nonlinear transconductor can be used the only restriction is that all the transconductors should have the same nonlinearity.

For example a linear current mirror can be designed using MOS transistors. It is necessary for the MOS transistors to have equal threshold voltages in order to have the same nonlinearity. The nonlinearity for a MOS transconductor, operating in saturation, is given by

$$i = \frac{\beta}{2} (V_{GS0} + v - V_T)^2 = \underbrace{\frac{\beta}{2} (V_{GS0} - V_T)^2}_{I_0} \underbrace{\left(1 + \frac{v}{V_{GS0} - V_T}\right)^2}_{f(v)} = I_0 f(v) \quad (1.11)$$

in this equation  $V_{GS0}$  is the quiescent gate-source voltage and  $v$  is the signal voltage.

### 1.2.2 Current Memories

A current memory is a circuits element capable of storing a current. To store a current we have to convert it to a voltage that then can be stored on a capacitor. For converting the current to a voltage we will make use of a transconductor. Two different methods for storing a current will be described, a 1st generation current memory [5][6][7][8][9][10][11][12] and a 2nd generation current memory (current copier) [13][14][15][16][17][18][7][19][20]. In Fig. 1.5

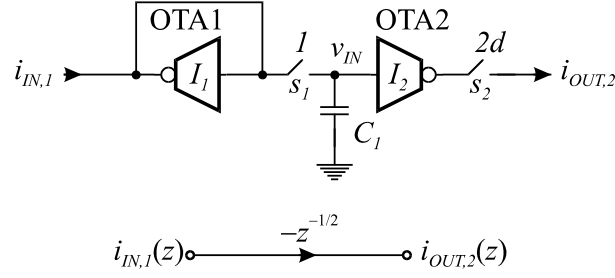


Figure 1.5: 1st generation current memory and the corresponding signal flow graph (SFG).

we have a first generation current memory it is basically a traditional current mirror with a switch. Multiple outputs are possible by connecting more than one transconductor to the voltage  $v_1$ . It operates as follows: OTA1 is used for converting the input current  $i_{IN,1}$  to a voltage  $v_{IN}$ . This voltage is then, on clock phase 1 when switch  $S_1$  is closed, applied to the capacitor  $C_1$ . When switch  $S_1$  is opened the voltage  $v_{IN}$  is stored on the capacitor  $C_1$ , and is then converted back to a current by the transconductor OTA2.

On clock phase 1 we have that:

$$i_{IN,1} = I_1 f(v_{IN}) \Leftrightarrow v_{IN} = f^{-1}\left(\frac{i_{IN,1}}{I_1}\right) \quad (1.12)$$

and on clock phase 2 we have that:

$$i_{OUT,2} = -I_2 f(v_{IN}) = -I_2 f\left(f^{-1}\left(\frac{i_{IN,1}}{I_1}\right)\right) = -i_{IN,1} \frac{I_2}{I_1} \quad (1.13)$$

So this kind of current memory has a optional scaling determined by  $-I_1/I_2$ . The accuracy of this scaling will be determined by how accurate the two transconductors can be matched. As with the current mirror we only get a linear operation if the transconductors have the same nonlinearity.

If we use the same transconductor for converting the signal current to a voltage and the voltage back to a signal current we can avoid any matching problems and we also ensure that the nonlinearity is the same which results in a higher linearity. Such a circuit is shown in Fig. 1.6. In Fig. 1.6 we have a second generation current memory. It operates as follows:

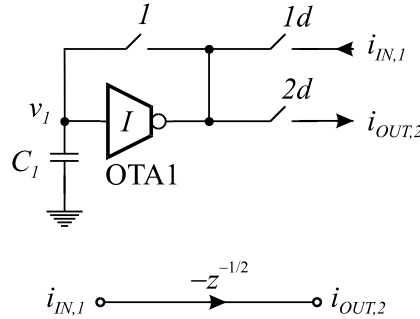


Figure 1.6: 2nd generation current memory (Current Copier) and the corresponding signal flow graph (SFG).

OTA1 is used both for converting the input current to a voltage and for converting the voltage back to a current.

On clock phase 1 we have that:

$$i_{IN,1} = If(v_1) \Leftrightarrow v_1 = f^{-1}\left(\frac{i_{IN,1}}{I}\right) \quad (1.14)$$

and on clock phase 2 we have that:

$$i_{OUT,2} = -If(v_1) = -If\left(f^{-1}\left(\frac{i_{IN,1}}{I}\right)\right) = -i_{IN,1} \frac{I}{I} = -i_{IN,1} \quad (1.15)$$

So the 2nd generation current memory has a scaling factor of  $-1$ . It is very accurate because it does not depend upon matching of different transconductors. However if we want multiple current outputs we have to connect the other transconductors to the voltage  $v_1$ . The output current from these extra outputs will have the same accuracy limitations as for the 1st generation current memory.

All of the current memory circuits described in this chapter utilize a two phase nonoverlapping clock scheme. All switches that connect directly to a storage capacitor operate either on clock phase 1 or 2. All other switches operate on clock phases  $1d$  or  $2d$ , where  $d$  denotes a small delay. This notation can be seen in Fig. 1.5 and Fig. 1.6. The timing of the clock phases is shown in Fig. 1.7. This clock scheme insures that the voltage held on the storage

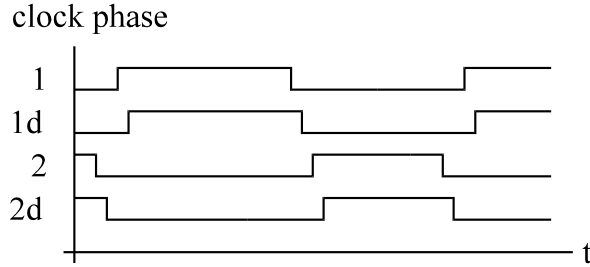


Figure 1.7: Timing of the clock phases used in the current memories

capacitors represents the correct input current and that it is not influenced by errors induced from the other switches in the circuit.

In order to make the circuits more readable the delay  $d$  is not necessary explicitly shown in the circuits (see Fig. 1.8 and Fig. 1.9).

### 1.2.3 Sample Delay

The operation of the current copier is basically an inverting half sample delay  $-z^{-1/2}$ . In order to generate a whole sample delay  $z^{-1}$  we can simply cascade two current copiers as shown in Fig. 1.8. The transfer function of this sample delay is easily seen from the SFG as

$$H(z) = (-z^{-1/2}) \cdot (-z^{-1/2}) = z^{-1} \quad (1.16)$$

#### Example 1.2.1

An implementation of the sample delay in Fig. 1.8, using simple current sources and transconductors, is shown in Fig. 1.9. A simulation of the sample delay shown in Fig. 1.9 has been performed for a single current pulse at the input with a duration of one clock period. The simulation was performed using the parameters shown in Table 1.1. From the simulation results in Fig. 1.10 we see that the relative error of the current pulse at the output of the sample delay is:

$$\epsilon = 1 - \frac{9.689\mu A}{10\mu A} = 1 - 0.9689 = 0.0311 \sim 3.1\% \quad (1.17)$$

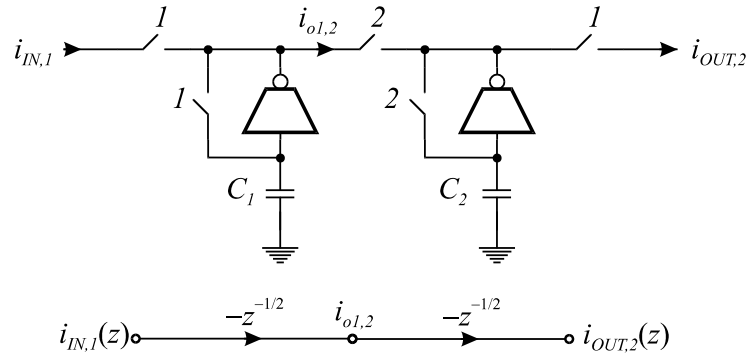


Figure 1.8: Sample delay using cascading of two current copiers and its corresponding SFG.



Figure 1.9: Implementation of a sample delay using single MOS transistors as transconductors.

This is indeed a large error that in most practical situation would be unacceptable. From this we conclude that it is necessary to identify the error sources and enhance the circuits in order to reduce the errors so that the circuits can be used. This will be the subject of the next chapter. ■

Table 1.1: Parameters used in the simulation of the implemented sample delay

Parameter	Value
$I$	$20\mu A$
$i_{IN}$	$10\mu A$
$\Delta v_1 = \Delta v_2$	$0.47v$
$C_1 = C_2$	$10pF$
$f_s$	$512kHz$

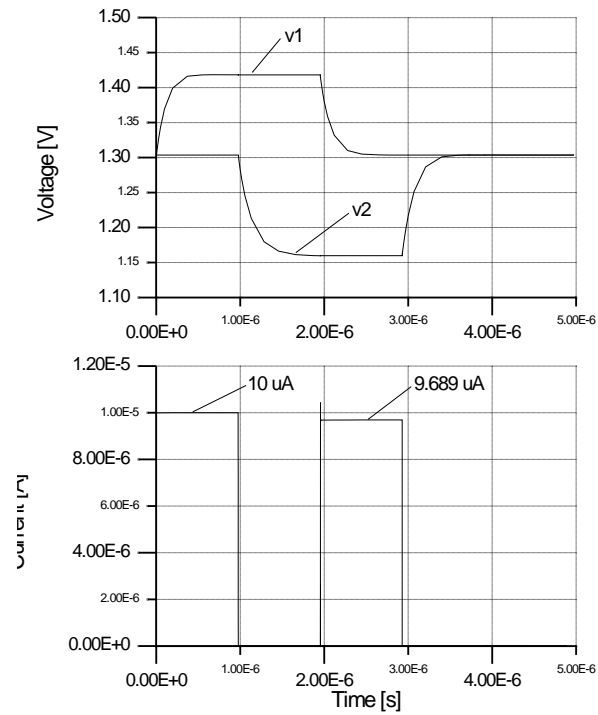


Figure 1.10: Simulation of the implemented sample delay for a single input current pulse