Switched Current Circuits

Design, Optimization and Applications

by

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Preface

This thesis is the result of the research I did on Switched Current Circuits. The work was carried out, at the Electronics Institute at the Technical University of Denmark, in the period September 1, 1992 to February 28, 1995.

This thesis consists of 17 chapters grouped into four major parts: Theory, Applications, Appendices and Publications.

The Theory part treats both basic and advanced topics of switched current circuits. In this part we show how basic sampled data systems can be build using Switched Capacitor (SC) and Switched Current (SI) techniques. We also identify the limiting factors in SI circuits and show how to design enhanced current copiers that overcome some of those limitations. Then we show how current copiers can be put together in order to build some of the basic building blocks used in many practical applications e.g. sample delays, delay lines, integrators and differentiators. We also discuss some more advanced topics such as nonlinear settling errors and optimization.

The Applications part gives examples of switched current circuits that have been implemented in silicon. This part covers topics such as filters, serial A/D and D/A converters, Sigma-Delta modulators and adaptive filters.

The Appendices part covers topics such as sampling of noise, current transmission errors and switching transients, matching and MOS transconductors. The presentation of these topics is done so they easily fit into the Theory part of this thesis.

The Publications part is an collection of enclosed copies of the papers that I have published during my Ph.D. study.

Examples

The text in this thesis contains several examples that are used to illustrate some ideas, concepts and circuits. The examples are recognized as sections of text having the following layout.

Example 0.0.1
This is an example of an example. Please notice that the end of all examples is marked with a small black box. ■

Acknowledgments

I would like to thank Thomas Kaulberg for a pleasant and enjoyable cooperation on the MAGFET project and for many valuable discussions regarding current mode circuits and techniques.

I would also like to thank Ivan Harald Holger Jørgensen for an enjoyable cooperation on the Adaptive filter project and for doing a tremendous job on the layout of the adaptive

filter. I'am also very grateful to Ivan for doing a thorough proof reading the manuscript for this thesis.

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Also I would like to thank OTICON, DANAVOX, MICROTRONIC and DELTA for their interest in my work.

Typesetting

This thesis has been typeset using LaTeX 2_ε in an 11pt Computer Modern Font. All of the figures have been prepared using **CorelDraw** and **Grafer4Windows** and the figures were inserted into the text as Windows-Meta-Files (WMF) using the `\special` command. The bibliography was generated using BibTeX and the printing of this thesis was performed using the Windows DVI viewer **DviWin**.

Gudmundur Bogason
Frederiksberg, September 4, 1995

Abstract

English

This thesis focuses mainly on SI circuits. The treatement of the SI technique is most of the time kept on a high level using transconductors instead of transistor. It is the authors believe that this results in an easier and clearer understanding of the operation of the SI circuits because the circuits are not cluttered with confusing transistors circuits. When needed, transistor circuits are presented in order to show specific implementation details or novel circuitry.

Basic techniques for sampled data system design is presented, and it is shown that linear signal processing functions using nonlinear components in both SI and SC techniques are feasible and that they rely on the same common principles.

The design of current copiers and sampled data building blocks is presented in details, this applies to both single ended and differential circuits. The limitations found in current copiers are discussed and novel new implementations of SI building blocks are presented.

The effect of nonlinear settling errors on the operation of SI circuits is illustrated and it is shown that nonlinear settling errors are caused by the nonlinear transconductors used in the current copier cells. Simulations are presented that show that the effect of the nonlinear settling is an increase in Total-Harmonic-Distortion (THD) with the frequency of the signals. Techniques for reduction of the nonliear settling errors are outlined and it is shown that highly linear SI circuits require the use of linear transconductors and high bandwidth (large bias current).

Optimization of SI circuits with regards to noise properties is presented and an optimization methology is outlined that can be used to optimize SI circuits for minimum power consumption for a given Signal-To-Noise-Ratio (SNR). This optimization methology has further been used in the design of two Sigma-Delta modulators and in the design of an adaptive filter. It is shown that circuits operating in weak inversion are not feasible for the SI technique because of the limited voltage swing found in these circuits.

Practical applications of the SI technique are presented and it is demonstrated that high order filters with good tracking between highpass and lowpass sections, using only MOS transistors and gate-capacitors, are feasible. Also, a serial A/D and D/A conversion system is presented that is capable of offset compensating and converting the current from a MAGFET[1] transistor to a seven bit digital value. This system is implemented in a $1.5\mu m$ digital CMOS process using only MOS transistors. An adaptive filter with 96 filter taps is implemented in SI technique. The filter is designed to estimate the transfer function of a micromechanical flow channel in order to estimate the flow rate of a fluid flowing in that channel. Also, the design of two Sigma-Delta modulators is presented and a brief discussion of high order modulators is given.

[1] MOS transistor sensitive to a magnetic field

Dansk

Denne afhandling omhandler hovedsageligt SI kredsløb. Gennemgangen af SI teknikken er for det meste holdt på et overordnet niveau, ved brug af transkonduktans forstærkere istedet for transistorer. Det er forfatterens overbevisning, at dette vil lette forståelsen for hvordan SI kredsløbene fungerer, fordi kredsløbene ikke bliver forvirrede af uoverskuelige transistor kredsløb. Når det er nødvendigt, anvendes specifikke transistor kredsløb for at illustrere implementerings detaljer og nye kredsløbs koblinger.

Grundlægende teknikker for tidsdiskrete analoge kredsløb er præsenterede og det bliver vist at lineære signal behandlings funktioner v.h.a. ulineære komponenenter i både SI og SC teknik er mulige, og at de er baserede på de samme grundlæggende principper.

Design af current copiers og tidsdiskrete byggeblokke bliver præsenteret i detaljer, dette gælder både for almindelige og differentielle kredsløb. De begrænsninger der ligger i current copiers bliver diskuterede og nye implementeringer af SI byggeblokke bliver præsenteret.

Effekten af ikke lineære settling fejl på funktionen af SI kredsløb er illustreret og det bliver vist at ulineære settling fejl skyldes de ulineære transkonduktans forstærkere, der bliver brugt i current copier cellerne. Der bliver præsenteret simuleringer, der viser at effekten af ulineære settling fejl er en stigning af den harmoniske forvrængning (THD) med frekvensen af signalet. Teknikker til reduktion af de ulineære settling fejl bliver skitseret og det bliver vist, at meget lineære SI kredsløb kræver at man bruger lineære transkonduktans forstærkere og høj båndbredde.

Optimering af SI kredsløb m.h.t. støj egenskaber bliver præsenteret, og en optimerings metode bliver skitseret, som kan bruges til at optimere SI kredsløb for et minimalt effekt forbrug for et givet signal støj forhold (SNR). Denne optimerings metode er endvidere blevet brugt til design af to Sigma-Delta modulatorer, og til design af et adaptivt filter. Det bliver vist at kredsløb der fungerer i weak-inversion ikke er velegnede til SI kredsløb p.g.a. det begrænsede spændings sving i disse kredsløb.

Praktiske anvendelser af SI teknikken bliver præsenteret, og det bliver demonstreret at højere ordens filtre med god tracking mellem højpas og lavpas sektionerne er mulige, alene baseret på MOS transistorer og gate-capaciteter. Også et serielt A/D og D/A konverterings system bliver presenteret, der er i stand til at offset kompensere, og konvertere strømmen fra en MAGFET[2] transistor til et syv bit tal. Systemet er implementeret i en $1.5\mu m$ digital CMOS process, alene v.h.a. MOS transistorer. Et adaptivt filter med 96 filter koefficienter er blevet implementeret i SI teknik. Filteret er beregnet til at estimere overførings funktionen af en mikromekanisk flow kanal for at man skal kunne estimere flow hastigheden af en væske i flow kanalen. Der bliver også presenteret to Sigma-Delta modulatorer, og der bliver givet en kort diskusion af højre ordens modulatorer.

[2] en MOS transistor der er følsom overfor et magnetisk felt

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List of Abbreviations

SI	Switched - Current.
SC	Switched - Capacitor.
CCII−	Second generation Current Conveyor, minus type.
CCII+	Second generation Current Conveyor, plus type.
OTA	Operational Transconductance Amplifier.
VOA	Voltage Mode Operational Amplifier.
COA	Current Mode Operational Amplifier.
CFB	Current Feedback Amplifier.
CCOP	Current Copier.
CM	Current Mirror.
MOS	Metal Oxide Semiconductor.
A/D	Analog to Digital.
D/A	Digital to Analog.
MSB	Most Significant Bit.
LSB	Least Significant Bit.
MASH	Multistage Noise Shaping.
SDM	Sigma-Delta Modulator.
$\Sigma\Delta$	Sigma-Delta.
SFG	Signal Flow Graph.
VLSI	Very Large Scale Integration.
CMR	Comonmode Regulation.
CMRR	Comonmode Rejection Ratio.
PSRR	Power Supply Rejection Ratio.
MPW	Multi Project Wafer.
FSM	Finite State Machine.

List of Notations

Physical paramers

Oxide thicknes.

$$t_{OX}$$

Oxide capacitance per area.

$$C'_{OX} = \frac{\epsilon_{S_i}}{t_{OX}}$$

mobility.

$$\mu$$

Transconductance parameter.

$$K' = \mu C'_{OX}$$

MOS transistor paramers

Channel width.

$$W$$

Channel length.

$$L$$

Transconductance parameter.

$$\beta = \frac{W}{L} K'$$

Thresshold Voltage.

$$V_T$$

Gate-Source Voltage

$$v_{GS}$$

Drain-Source Voltage

$$v_{DS}$$

Saturation voltage.

$$\Delta v = V_{GS} - V_T$$

Signal analysis

Sequence.

$$x[n]$$

Finite length sequence.

$$x[n], 0 \leq n \leq N-1$$

Matrix and Vector.

$$\mathbf{x}$$

Transposed.

$$\mathbf{x}^T$$

Conjugate.

$$\mathbf{x}^*$$

Finite length sequence as vector.

$$\mathbf{x} = \begin{bmatrix} x[0] \\ x[1] \\ \vdots \\ x[N-1] \end{bmatrix}$$

Analog autocorrelation.

$$R_x(\tau)$$

Analog power spectral density.

$$S_x(f)$$

Sampled analog autocorrelation.

$$r_x(\tau)$$

Sampled analog power spectral density.

$$s_x(f)$$

Digital autocorrelation.

$$r_x[m]$$

Digital power spectrum.

$$s_x(e^{j2\pi f \Delta T})$$

Fourier pair.

$$g(t) \leftrightarrow G(f)$$

Analog Fourier transform.

$$G(f) = \int_{-\infty}^{+\infty} g(t) e^{-j2\pi f t} dt$$

Inverse Analog Fourier transform.

$$g(t) = \int_{-\infty}^{+\infty} G(f) e^{j2\pi f t} df$$

Analog Convolution.

$$g_1(t) \otimes g_2(t) = \int_{-\infty}^{+\infty} g_1(\theta) g_2(t-\theta) d\theta$$

$$g_1(t)g_2(t) \leftrightarrow G_1(f) \otimes G_2(f)$$
$$g_1(t) \otimes g_2(t) \leftrightarrow G_1(f)G_2(f)$$

Digital Fourier transform.

$$G(f) = \sum_{n=-\infty}^{+\infty} g[n]e^{-j2\pi fn\Delta T}$$

Inverse Digital Fourier transform.

$$g[n] = \frac{1}{f_S}\int_{-f_S/2}^{+f_S/2} G(f)e^{j2\pi fn\Delta T}df$$

Discrete Fourier Transform.

$$G[m] = \frac{1}{N}\sum_{n=0}^{N-1} g[n]e^{-jmn\frac{2\pi}{N}}$$

Inverse Discrete Fourier Transform.

$$g[n] = \sum_{m=0}^{N-1} G[m]e^{jmn\frac{2\pi}{N}}$$

Introduction

The development of integrated circuit processing technology has now reach a stage where it is possible to integrate several millions transistors on a single chip. Chip's containing approximately 10 million transistors have been reported.

Processing technology is being tuned for optimum performance for digital circuits. This implies shrinking device sizes for increasing speed and lowering the supply voltage for reduced power consumption.

It is mainly digital circuits that have gained most from the evolving processing technology. It is therefore natural to se more and more signalprocessing function performed digitally.

Large analog chip's are rare now at days. The analog circuitry is now mostly used for interfacing the digital circuits to the outside world. The main functions for analog circuits, in mixed mode designs, are therefore data conversion and filtering.

Traditionally switched capacitor (SC) circuits have been used extensively in the analog interface portion of mixed mode integrated circuits. They have been used for filtering , A/D and D/A conversion and many other interfacing functions.

Switched current (SI) circuits have recently been proposed as a possible replacement or an alternative to SC circuits in mixed mode designs. The motivation for this has been that processing technology is being tuned for digital designs implying that there might be no good analog components left such as: large double poly capacitors etc. which normally are required in SC circuits.

Also, it has often been said that SI circuits can be designed using modest circuitry, i.e. only MOS transistors and nonlinear capacitors e.g. gate-source capacitors, which of course make SI circuits perfect for digital CMOS processes.

In this thesis I will show that the above statements are only true with some slight modifications. It will be shown that linear SC circuits can be designed using nonlinear capacitors, making SC circuits compatible with digital CMOS processes and that high performance SI circuits do require the same circuit complexity as SC circuits.

The main objective of this thesis is to investigate techniques for design of SI circuits with performance comparable to SC circuits. This implies that we look at different current copier cells and how to enhance them, it also implies that we look at noise in SI circuits and how to design for low power and low noise. Also, because SI circuits are inherently nonlinear we look at how nonlinear settling affects the operation of SI circuits.

Switched capacitor circuits can in most cases be analyzed as being linear circuits and there exists a lot of different design and analysis tools for SC circuits. There is however one crucial difference between SC and SI circuits. SI circuits are inherently nonlinear. Because of this difference it is necessary to use different design tools to make full use of the SI technique. Some efforts have been made to designing tools for SI circuits, but all of these tools assume that SI circuits are linear. Until now the only tool available for simulating nonlinearities in SI circuits has been SPICE.

As long as small circuits are being analyzed, such as current copiers etc., it is possible to use SPICE, but for moderately large SI circuits such as Sigma-Delta Modulators it is not feasible to use SPICE for simulating the effect of nonlinearities in the SI circuits because of the excessively long simulation time.

Because of these limitations, I have in this thesis combined several tools, in order to cope with the complexity and simulation requirements of the SI circuits. Some of these tools are: PSPICE, which is used for detailed circuit level simulation, although it sometimes results in excessive simulation times. C++, which is used for behavioral level simulations, making it possible to simulate the effect of nonlinear settling errors on large SI circuits. MATLAB, which is used for optimization of SI circuits and for post processing of simulation results.

Part I

Theory

Chapter 1

Basic Techniques for Sampled Data Systems

The aim of this chapter is to introduce the most basic building blocks used in most analog sampled data systems today i.e. switched–capacitor [1][2][3] and switched–current circuits. The main point in this introduction will be to show that both SC and SI circuits are compatible with digital CMOS processes (single Poly processes), i.e. CMOS processes that do not support large linear floating capacitors, and that linear analog sampled data systems can easily be built using nonlinear capacitors (voltage dependent) in the SC case and using nonlinear transconductors and capacitors in the SI case.

This chapter also introduces signal flow graphs (SFG) as an powerful tool for analyzing and synthesizing SI circuits. It is assumed that the reader is familiar with the notation of z-transforms as it is the fundamental tool for describing sampled data systems just as laplace-transform is used for describing continuous-time circuits.

1.1 Switched Capacitor Circuits using Nonlinear Capacitors

It is well known that linear scaling of signal currents is possible using current mirrors, that are based on transconductors with a nonlinear relationship between the input voltage and the output current (MOS transistors). In a similar way it is also possible to design switched capacitor (SC) circuits performing linear signal processing using nonlinear capacitors. This can be done by using charge mirrors [4].

The consequence of this fact is that linear SC filters can be implemented without the need for double Poly processes i.e. they can be implemented in digital CMOS processes.

In order to illustrate the operation of the charge mirror, we will assume that the capacitors that are voltage dependent have the following relationship between capacitance and voltage.

$$C = C(v) = C_0(1 + c_1 v + c_2 v^2) \tag{1.1}$$

here C_0 is the zero voltage capacitance and v is the applied voltage on the capacitor. The coefficients c_1 and c_2 represents the degree of nonlinearity. This type of voltage dependence is implemented in SPICE exactly as shown in the above equation. When a capacitor has a voltage dependence as shown in the above equation, the orientation of the capacitor becomes important if the voltage dependence contains odd order terms such as c_1.

The current through the capacitor is found as the derivative of the voltage times the

capacitance

$$i = C\frac{dv}{dt} = C_0(1 + c_1 v + c_2 v^2)\frac{dv}{dt} = C_0\left(\frac{dv}{dt} + \frac{1}{2}c_1\frac{d(v^2)}{dt} + \frac{1}{3}c_2\frac{d(v^3)}{dt}\right) \tag{1.2}$$

The charge on the nonlinear capacitor can be found by integrating the current through the capacitance

$$q = \int i\ dt = C_0\left(v + \frac{1}{2}c_1 v^2 + \frac{1}{3}c_2 v^3\right) = C_0 f(v) \tag{1.3}$$

From this equation we see that the charge on a nonlinear capacitor can in general terms be represented as some zero voltage capacitance C_0 multiplied by a nonlinear function $f(v)$ of the applied voltage.

1.1.1 Charge Scaling

If we want to perform linear signal processing of charges we can do that utilizing charge mirrors. A charge mirror capable of performing linear charge scaling, using nonlinear capacitors, is shown in Fig. 1.1. Please note that the orientation of the nonlinear capacitor is explicitly shown with the plus (+) and minus (−) signs. The operation of the charge mirror shown in

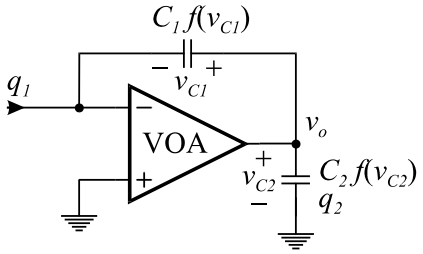

Figure 1.1: Linear charge mirror utilizing nonlinear capacitors

Fig. 1.1 can be described in the following way: The input charge q_1 enters the inverting input of the operational amplifier and is put on the capacitor C_1 this gives the following voltage across the capacitor C_1

$$-q_1 = C_1 f(v_{C_1}) \Leftrightarrow v_{C_1} = f^{-1}(\frac{-q_1}{C_1}) \tag{1.4}$$

Assuming that the operational amplifier is ideal, i.e. the voltage at the negative input (-) is zero (Virtual Ground), the voltage at the output of the operational amplifier is given by

$$v_0 = v_{C_1} = f^{-1}(\frac{-q_1}{C_1}) \tag{1.5}$$

this voltage is applied to the capacitor C_2, which gives a charge of

$$q_2 = C_2 f(v_0) = C_2 f(f^{-1}(\frac{-q_1}{C_1})) \tag{1.6}$$

the function of the inverse function, $f(f^{-1}(\cdot)) = (\cdot)$, cancels out and we end up with the following relationship for the charge transfer

$$q_2 = -q_1\frac{C_2}{C_1} \tag{1.7}$$

This shows that the circuit will act as a inverting linear charge mirror, with a mirroring factor determined by the ratio between the zero voltage capacitors. The constraint for getting linear charge transfer is that the two capacitors C_1 and C_2 must have the same voltage dependence $f(\cdot)$, and that they are orientated in a way so that their nonlinearities are adjacent as shown in Fig. 1.1.

Example 1.1.1
This example illustrates that it is possible to get a linear relationship between input charge and output charge using nonlinear capacitors. This example is based on the configuration shown in Fig. 1.1. The capacitors C_1 and C_2 have both the following nonlinearities: $c_1 = 2$ and $c_2 = 3$. Also the zero voltage capacitors are $C_1 = 10pF$ and $C_2 = 20pF$. The input

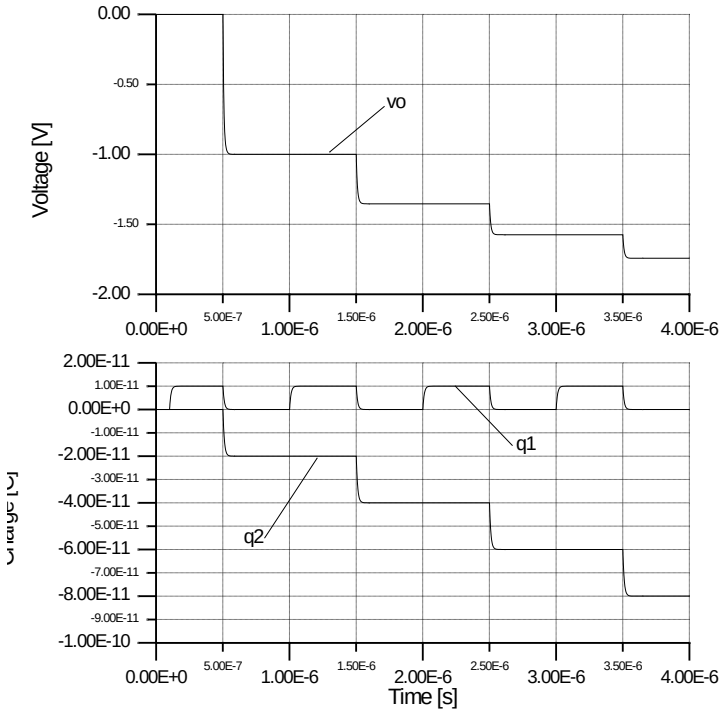

Figure 1.2: Relationship between input charge packets and output charge. Simulation performed using PSPICE

to the charge mirror is a periodic sequence of charge packages q_1 each carrying a charge of $10pC$. The charge packages are accumulated on the capacitor C_1, and this gives the output voltage v_o shown in Fig. 1.2. We notice that there is a nonlinear relationship between the output voltage v_o and the charge q_1.

Also in Fig. 1.2 we see the charge q_2 put on the capacitor C_2. We notice that for each charge package q_1 of $10pC$ entering the charge mirror, the charge on capacitor C_2 is decremented by $20pC$. This indicates that the circuit operates as an inverting charge mirror with a scaling factor of $C_2/C_1 = 20pF/10pF = 2$, as expected. ■

1.1.2 Integrator

Most switched capacitor circuits rely on the use of integrators. It is therefore of great interest to be able to design switched capacitor integrators using nonlinear capacitors. The circuit

in Fig. 1.3 shows how it is possible to perform linear signal processing utilizing non-linear capacitors. In Fig. 1.3 there are two linear capacitors C_1, C_4 and two nonlinear capacitors

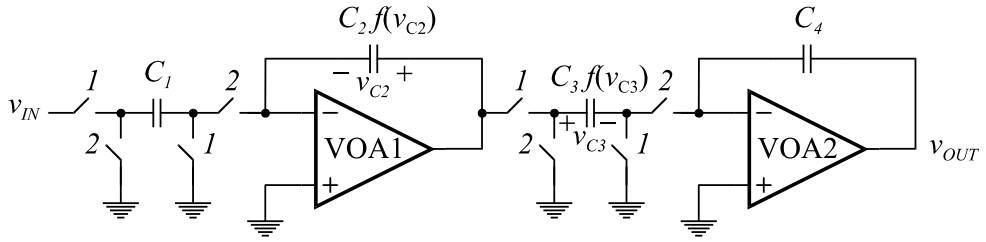

Figure 1.3: Cascade of two parasitic insensitive SC integrators utilizing nonlinear capacitors.

C_2, C_3. The linear capacitor C_1 is used to convert the input voltage v_{IN} to a linear charge q_1 on clock phase 1. This charge is then on clock phase 2 put on the nonlinear capacitor C_2. On clock phase 1 the nonlinear voltage at the output of operation amplifier VOA1 is placed on the nonlinear capacitor C_3, which then gets a charge corresponding to

$$q_2 = -q_1 \frac{C_2}{C_1} \tag{1.8}$$

as shown in the previous subsection on Charge Mirrors.

The first operational amplifier VOA1 together with the nonlinear capacitors C_2 and C_3 acts as a linear charge mirror. On clock phase 2 the linear charge on the nonlinear capacitor C_3 is put on the linear capacitor C_4, which in turn gives a linear output voltage at the output of operational amplifier VOA2.

1.2 Switched Current Circuits using Nonlinear Elements

The basic building blocks necessary for design of SI circuits are a switch, a grounded capacitor and an inverting transconductor. The capacitor and the transconductor do not have to be linear, although it will be shown later in Chapter 4, that in order to design SI circuits with low distortion it is necessary to consider the nonlinearities in the SI circuit elements.

The switch used in a SI circuit can be a NMOS,PMOS or CMOS switch depending on the actual implementiation and on the use of the switch. The capacitor can be the gate-source capacitance C_{GS} of a MOS transistor or it can be some other capacitor probably a MOS transistor coupled as a MOS capacitor. The transconductor can be build using a variety of configuration depending upon the application of the SI circuit. It can be a simple single transistor transconductor (Most often used for illustration) or it can be more complex using variety of cascoding arrangements for enhancing the performance. It can also be both single ended or fully differential and operating in class A or class AB. Different implementations of SI circuits will be described in Chapter 2 and Chapter 3.

The operation of SI circuits is based on the conversion of a signal current to a corresponding signal voltage, using a transconductor. The signal voltage can then be stored on a capacitor for later use, where it then is converted back to a signal current using a transconductor. The transconductors used for converting the signal current to a voltage and then back to a signal current again needs not be the same.

1.2.1 Current Scaling

All signal processing operations rely on the possibility of amplification or signal scaling of some sort. In switched current circuits we want to be able to amplify and scale signal currents. This operation is basically done using current mirrors. In Fig. 1.4 OTA0 is used

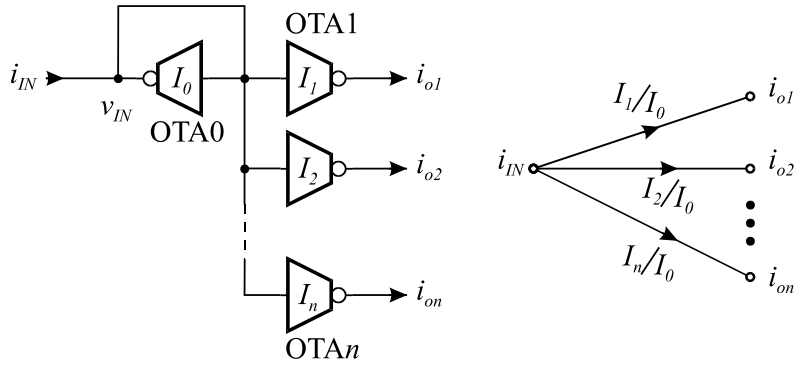

Figure 1.4: Current Mirror used for amplification or scaling of signal currents and the corresponding signal flow graph (SFG).

for converting the input current i_{IN} to a voltage v_{IN} that is applied to the inputs of the transconductors OTA1 to OTAn. Each transconductor contains a current I_n that represents the scaling factor of nonlinear transconductor. We have that:

$$i_{IN} = I_0 f(v_{IN}) \Leftrightarrow v_{IN} = f^{-1}(\frac{i_{IN}}{I_0}) \tag{1.9}$$

and the output current from transconductor i is given by:

$$i_{oi} = -I_i f(v_{IN}) = -I_i f(f^{-1}(\frac{i_{IN}}{I_0})) = -i_{IN}\frac{I_i}{I_0} \tag{1.10}$$

So the current at output i will have a scaling factor of $-I_i/I_0$. We observe that in order to get a linear current scaling any nonlinear transconductor can be used the only restriction is that all the transconductors should have the same nonlinearity.

For example a linear current mirror can be designed using MOS transistors. It is necessary for the MOS transistors to have equal threshold voltages in order to have the same nonlinearity. The nonlinearity for a MOS transconductor, operating in saturation, is given by

$$i = \frac{\beta}{2}(V_{GS0} + v - V_T)^2 = \underbrace{\frac{\beta}{2}(V_{GS0} - V_T)^2}_{I_0}\underbrace{\left(1 + \frac{v}{V_{GS0} - V_T}\right)^2}_{f(v)} = I_0 f(v) \tag{1.11}$$

in this equation V_{GS0} is the quiescent gate-source voltage and v is the signal voltage.

1.2.2 Current Memories

A current memory is a circuits element capable of storing a current. To store a current we have to convert it to a voltage that then can be stored on a capacitor. For converting the current to a voltage we will make use of a transconductor. Two different methods for storing a current will be described, a 1st generation current memory [5][6][7][8][9][10][11][12] and a 2nd generation current memory (current copier) [13][14][15][16][17][18][7][19][20]. In Fig. 1.5

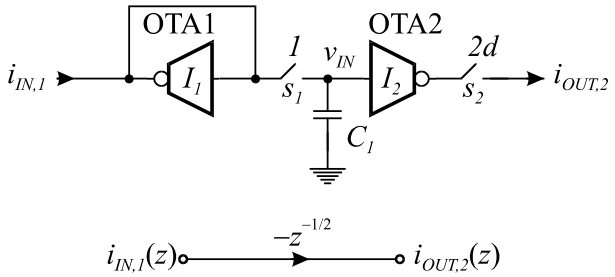

Figure 1.5: 1st generation current memory and the corresponding signal flow graph (SFG).

we have a first generation current memory it is basically a traditional current mirror with a switch. Multiple outputs are possible by connecting more than one transconductor to the voltage v_1. It operates as follows: OTA1 is used for converting the input current $i_{IN,1}$ to a voltage v_{IN}. This voltage is then, on clock phase 1 when switch S_1 is closed, applied to the capacitor C_1. When switch S_1 is opened the voltage v_{IN} is stored on the capacitor C_1, and is then converted back to a current by the transconductor OTA2.

On clock phase 1 we have that:

$$i_{IN,1} = I_1 f(v_{IN}) \Leftrightarrow v_{IN} = f^{-1}(\frac{i_{IN,1}}{I_1}) \tag{1.12}$$

and on clock phase 2 we have that:

$$i_{OUT,2} = -I_2 f(v_{IN}) = -I_2 f(f^{-1}(\frac{i_{IN,1}}{I_1})) = -i_{IN,1}\frac{I_2}{I_1} \tag{1.13}$$

So this kind of current memory has a optional scaling determined by $-I_1/I_2$. The accuracy of this scaling will be determined by how accurate the two transconductors can be matched. As with the current mirror we only get a linear operation if the transconductors have the same nonlinearity.

If we use the same transconductor for converting the signal current to a voltage and the voltage back to a signal current we can avoid any matching problems and we also ensure that the nonlinearity is the same which results in a higher linearity. Such a circuit is shown in Fig. 1.6. In Fig. 1.6 we have a second generation current memory. It operates as follows:

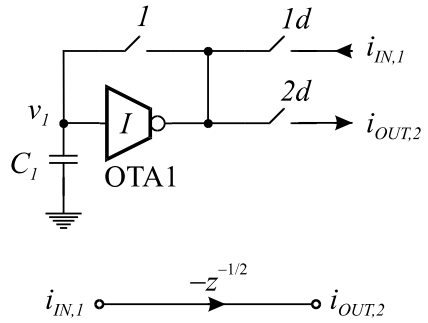

Figure 1.6: 2nd generation current memory (Current Copier) and the corresponding signal flow graph (SFG).

OTA1 is used both for converting the input current to a voltage and for converting the voltage back to a current.

On clock phase 1 we have that:

$$i_{IN,1} = If(v_1) \Leftrightarrow v_1 = f^{-1}(\frac{i_{IN,1}}{I}) \tag{1.14}$$

and on clock phase 2 we have that:

$$i_{OUT,2} = -If(v_1) = -If(f^{-1}(\frac{i_{IN,1}}{I})) = -i_{IN,1}\frac{I}{I} = -i_{IN,1} \tag{1.15}$$

So the 2nd generation current memory has a scaling factor of -1. It is very accurate because it does not depend upon matching of different transconductors. However if we want multiple current outputs we have to connect the other transconductors to the voltage v_1. The output current from these extra outputs will have the same accuracy limitations as for the 1st generation current memory.

All of the current memory circuits described in this chapter utilize a two phase nonoverlapping clock scheme. All switches that connect directly to a storage capacitor operate either on clock phase 1 or 2. All other switches operate on clock phases $1d$ or $2d$, where d denotes a small delay. This notation can be seen in Fig. 1.5 and Fig. 1.6. The timing of the clock phases is shown in Fig. 1.7. This clock scheme insures that the voltage held on the storage

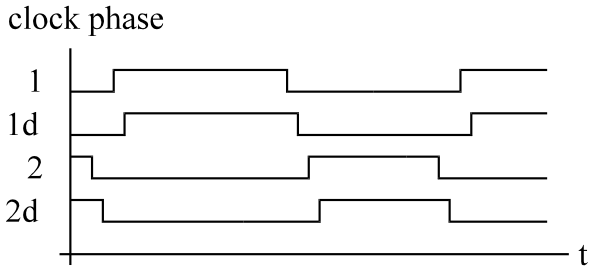

Figure 1.7: Timing of the clock phases used in the current memories

capacitors represents the correct input current and that it is not influenced by errors induced from the other switches in the circuit.

In order to make the circuits more readable the delay d is not necessary explicitly shown in the circuits (see Fig. 1.8 and Fig. 1.9).

1.2.3 Sample Delay

The operation of the current copier is basically an inverting half sample delay $-z^{-1/2}$. In order to generate a whole sample delay z^{-1} we can simply cascade two current copiers as shown in Fig. 1.8. The transfer function of this sample delay is easily seen from the SFG as

$$H(z) = (-z^{-1/2}) \cdot (-z^{-1/2}) = z^{-1} \tag{1.16}$$

Example 1.2.1
An implementation of the sample delay in Fig. 1.8, using simple current sources and transconductors, is shown in Fig. 1.9. A simulation of the sample delay shown in Fig. 1.9 has been performed for a single current pulse at the input with a duration of one clock period. The simulation was performed using the parameters shown in Table 1.1. From the simulation results in Fig. 1.10 we see that the relative error of the current pulse at the output of the sample delay is:

$$\epsilon = 1 - \frac{9.689\mu A}{10\mu A} = 1 - 0.9689 = 0.0311 \sim 3.1\% \tag{1.17}$$

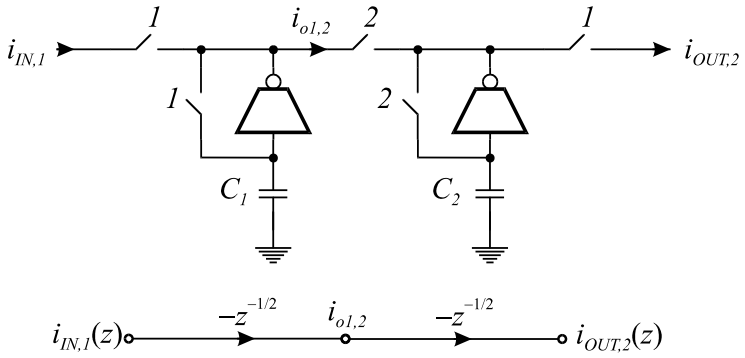

Figure 1.8: Sample delay using cascading of two current copiers and its corresponding SFG.

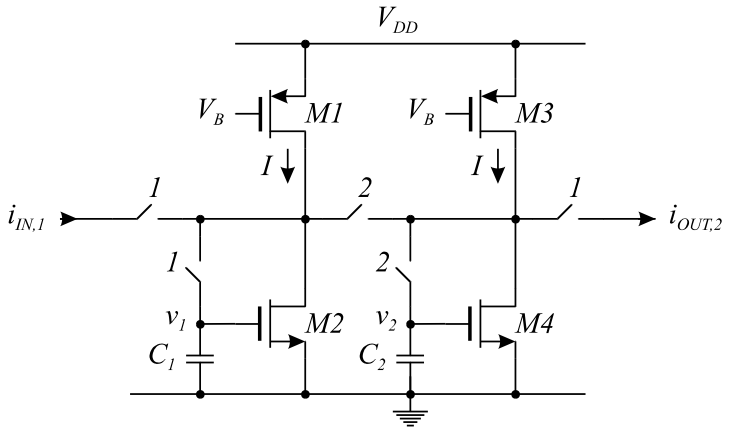

Figure 1.9: Implementation of a sample delay using single MOS transistors as transconductors.

This is indeed a large error that in most practical situation would be unacceptable. From this we conclude that it is necessary to identify the error sources and enhance the circuits in order to reduce the errors so that the circuits can be used. This will be the subject of the next chapter. ■

Table 1.1: Parameters used in the simulation of the implemented sample delay

Parameter	*Value*
I	$20\mu A$
i_{IN}	$10\mu A$
$\Delta v_1 = \Delta v_2$	$0.47v$
$C_1 = C_2$	$10pF$
f_s	$512kHz$

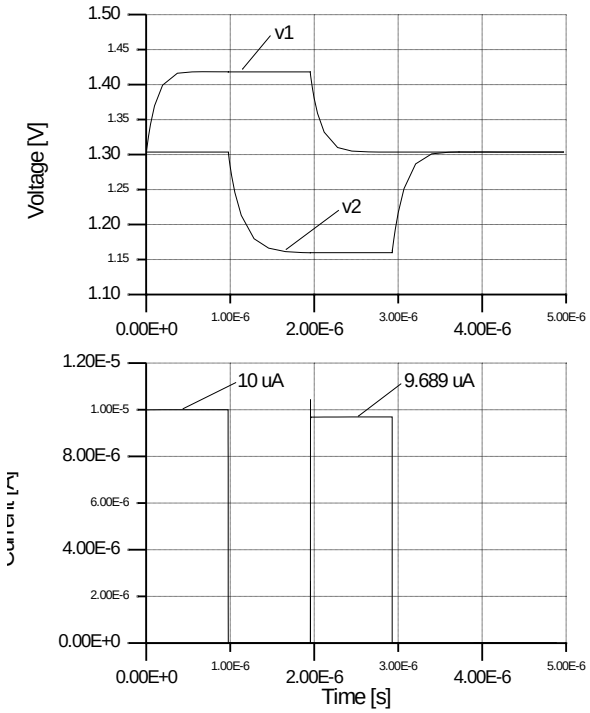

Figure 1.10: Simulation of the implemented sample delay for a single input current pulse