Chapter 10

Switched Current 3rd Order Sigma-Delta A/D Converter

This chapter describes the design and implementation of a 3rd order Sigma-Delta A/D Modulator. The modulator has been designed using fully differential switched current techniques, and implemented in an industry standard $2.4\mu m$ CMOS process using only MOS transistors and MOS capacitors.

The modulator was intended for audio applications, requiring a frequency band up to 22.05kHz. Operating with an oversampling factor of $R = 128$ this corresponds to a sampling frequency of 5.6448MHz.

This chapter gives a brief introduction to the subject of designing high order Sigma-Delta modulator. This introduction includes a discussion of stability problems, modulator topologies and modulator filter design.

10.1 Why use high-order modulators

It is well known that low order Sigma-Delta modulators i.e. modulators of order one and two are prone to generate tones in the audio band [37][38]. In audio applications these tones are unwanted and several attempts have been made for reducing these tones, e.g. by using chaos [40].

By increasing the modulator order, the tones become more chaotic and noise like [41][42][43]. It is also possible to reduce the tones by introducing large amount of dither signal at the input of the comparator, this however will reduce the stable input amplitude range of the modulator and reduce the SNR [43]. The tones can also be reduced by deliberately making the modulator chaotic [40], the effect of this is similar to the introduction of the dither signal [43].

10.2 Stability problems

Until recently it was generally believed that Sigma-Delta modulators of order higher than two were impossible to stabilize [44]. Therefore a lot of research went into developing different topologies based on 1st and 2nd order modulators [45]. One example of such a topology is the MASH (Multistage Noise Shaping) modulator [44].

Recently there has been a number of publications demonstrating the fact that it is indeed possible to design stable Sigma-Delta modulators with an order higher than three

[41][46][42][47][48]. A stable 8ht order Sigma-Delta D/A modulator, operating with an oversampling factor of 32, for high quality audio applications has been demonstrated [49][43].

When the modulator order is increased from 2nd order to a 3rd order or higher, the stability properties of the modulator change drastically [43]. This difference shows up in the way a modulator handles sudden overload conditions at the input.

It can be shown that modulators of order three and higher are only stable for a limited input signal range [43]. If the input signal should exceed the maximum stable amplitude (MSA) then it is very likely that the modulator will enter a unstable oscillating state [43]. The most annoying thing about this oscillating mode is that the oscillation are likely to be sustained even after the input signal is removed.

There are several ways for avoiding or reducing these sustained oscillations in high order modulators. One method is to introduce clamping at the outputs of the integrators used i the modulator filter. This will effectively limit the state space of the modulator and thereby reduce the possibility of the modulator entering a mode with sustained oscillations. Such a clamping scheme arises naturally in Sigma-Delta A/D modulators, because the modulator filter is a discrete time analog filter most often built using switched-capacitor or switched-current technology. Therefore the clamping will be set by the supply voltage or the bias current.

In Sigma-Delta D/A modulators, a natural clamping scheme similar to what is found in Sigma-Delta A/D modulators does not exist, although there is some limitation of the state space caused by wrap around effects in the arithmetic.

Simulations of Sigma-Delta A/D modulators have shown that it is very important to scale the signal levels in the modulator filter so that they are very close to be clamped when the input signal has its maximum value (MSA). This ensures that the modulator is very likely to avoid any sustained oscillations when overloaded.

Another possibility for reducing the sustained oscillations is to detect long sequences of high and low's in the output sequence of the modulator. Such sequences indicate the existence of a low frequency oscillation that might be present in the audio band. The oscillation can be stopped by resetting the integrators, when such a sequence is detected. This will also effectively limit the state space of the integrators used in the modulator filter [42].

10.3 Modulator topology

Several topologies exist for implementing the modulator filter [44][45][41][42], I have chosen the multiple feedback configuration [42][43]. This has been done because it is well suited for switched-current implementations as the feedback coefficients (DAC's) can be implemented as simple current switches.

It is however a little bit more complicated to implement multiple feed-input of the input signal, which can be used to decrease the internal signal swing in the integrators. This property is of great importance for switched-current implementations of sigma-delta modulators, because the power consumption will decrease if the maximum internal signal swing is decreased. The modulator topology chosen for this design is shown in Fig. 10.1. The modulator consist of three lossless noninverting one sample delay integrators with the transfer function: $1/(z-1) = z^{-1}/(1-z^{-1})$, three feedback coefficients b_1, b_2, b_3 that determine the noise shaping and the stability properties and two feed-input coefficients a_1, a_2 that are used for reducing the internal signal swing in the integrators. An optional signal path shown with doted lines can be included in the modulator. The effect of this signal path is to introduce a zero in the noise transfer function NTF(z), that can be optimally located for reducing the quantization noise in the signal band by 8dB [50].

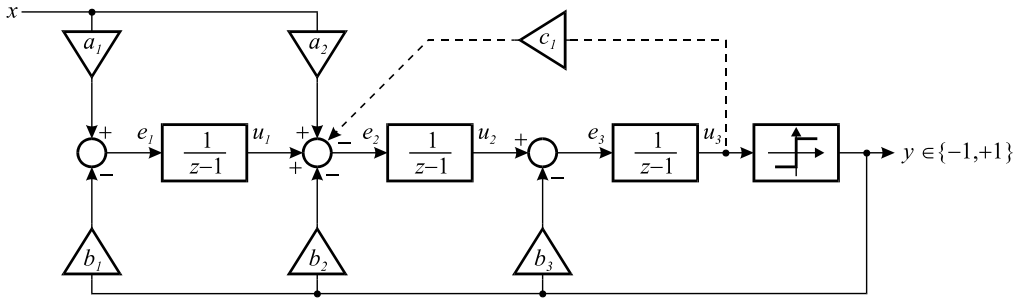

Figure 10.1: Modulator topology

For analyzing the modulator shown in Fig. 10.1 we will make use of the generic modulator shown in Fig. 10.2. This modulator is fully linear i.e. the quantizer is modeled as a noise gain of K_n plus some quantization noise q. By comparing Fig. 10.2 with Fig. 10.1 we se that

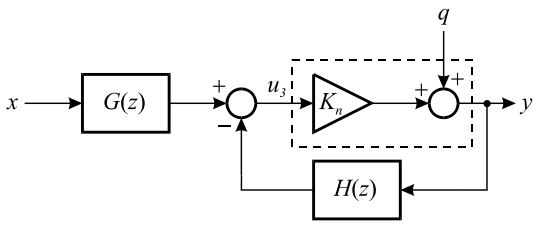

Figure 10.2: Generic Modulator with linearized quantizer

the input filter $G(z)$ and the feedback filter $H(z)$ can be written as

$$G(z) = \frac{U_3(z)}{X(z)} = \frac{a_1}{(z-1)^3} + \frac{a_2}{(z-1)^2} \tag{10.1}$$

$$H(z) = -\frac{U_3(z)}{Y(z)} = \frac{b_1}{(z-1)^3} + \frac{b_2}{(z-1)^2} + \frac{b_3}{(z-1)} \tag{10.2}$$

The generic Sigma-Delta modulator shown in Fig. 10.2 can be transformed into an equivalent noise-shaper structure as shown in Fig. 10.3. It is easily shown that this structure is

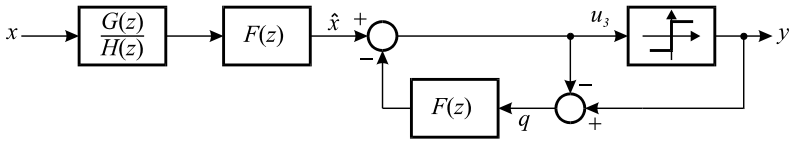

Figure 10.3: Noise-shaping modulator structure

equivalent to Fig. 10.2 if we choose the filter $F(z)$ according to the following equation.

$$F(z) = \frac{H(z)}{1 + H(z)} \tag{10.3}$$

The generic modulator shown in Fig. 10.2 and the equivalent noise-shaper modulator shown in Fig. 10.3 will be used for illustrating some important stability criterion.

10.4 Modulator filter and stability analysis

Using the generic modulator in Fig. 10.2 we get that the noise transfer function $\mathrm{NTF}_{K_n}(z)$ and the signal transfer function $\mathrm{STF}_{K_n}(z)$ can be written as

$$\mathrm{NTF}_{K_n}(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1 + K_n H(z)} \tag{10.4}$$

$$\mathrm{STF}_{K_n}(z) = \frac{Y(z)}{X(z)} = \frac{K_n G(z)}{1 + K_n H(z)} \tag{10.5}$$

These equations show that the quantization noise is highpass filtered and that the signal is lowpass filtered.

In order to simplify the design of the feedback filter $H(z)$ a prototype highpass filter is used for $\mathrm{NTF}_{K_n}(z)$. This reduces the number of free parameters to one, namely the cut-off frequency of the highpass filter. The choice of the cut-off frequency will affect the stability of the modulator and it also determines the maximum stable input amplitude (MSA).

When determining the feedback filter $H(z)$, the comparator gain K_n can arbitrarily be set to one, because any scaling of the feedback filter will be absorbed in the comparator [43].

Assuming that the quantization noise q is a white stochastic noise with zero mean and variance σ_q^2, the noise power at the output of the modulator, as a function of the comparator gain K_n, can be found by integrating (10.4).

$$\sigma_y^2 = \sigma_q^2 \frac{1}{f_s} \int_{-f_s/2}^{+f_s/2} |\mathrm{NTF}_{K_n}(f)|^2 df = \sigma_q^2 A(K_n) \tag{10.6}$$

The noise amplification $A(K_n)$ can also be found using Parsevals theorem

$$A(K_n) = \sum_{i=0}^{\infty} |\mathrm{ntf}_{K_n}(i)|^2 \tag{10.7}$$

Here $\mathrm{ntf}_{K_n}(i)$ is the impulse response sequence of the noise transfer function with a linearized comparator gain of K_n. By plotting $A(K_n)$ as a function of K_n we get a $\cup$-convex relationship for all higher order modulators i.e. all modulators of order 3 or higher. The value of $A(K_n)$ at the global minimum will be denoted by A_{min}.

Assuming that the input signal to the quantizer is gaussian it can be shown that the noise amplification $A(K_n)$ must fulfill the relationship [43]

$$A(K_n) = \frac{1 - m_y^2}{1 - m_y^2 - \frac{2}{\pi} e^{-2(\mathrm{erf}^{-1}(m_y))^2}} \tag{10.8}$$

where m_y is the mean output of the quantizer, and $\mathrm{erf}^{-1}(\cdot)$ is the inverse error function.

Because the modulator oversamples the input signal so heavily, the input signal to the modulator can be regarded as being a DC signal with an mean value of m_x. Assuming that the modulator has been scaled so that $b_1 = a_1$, we have that the mean output m_y from the quantizer is equal to the mean input m_x.

$A(K_n)$ is a decreasing function of m_y and we have that

$$A(K_n)|_{m_y=0} = \frac{\pi}{\pi - 2} \simeq 2.7519 \tag{10.9}$$

We can now conclude that the global minimum A_{min} of $A(K_n)$ must be smaller that 2.7519. Equation (10.8) shows that by increasing $|m_y|$ i.e. $|m_x|$ the noise amplification $A(K_n)$ decreases, when the noise amplification $A(K_n)$ reaches its global minimum A_{min}, the corresponding value of $|m_y|$ i.e. $|m_x|$ is called the maximum stable input amplitude MSA. When

the input amplitude exceeds MSA the modulator is very likely to become unstable. This is called the gaussian stability criterion [43].

The maximum obtainable signal-to-noise-ratio SNR is dependent upon the choice of MSA. If we design a modulator with a high MSA, the modulator will perform a poorer coding of the input signal leading to a reduced SNR. The optimum choice of MSA is approximately 0.4 [43].

Another stability criterion called the BIBO (Bounded Input Bounded Output) can be derived, based upon the Noise-shaper modulator shown in Fig. 10.3. The criterion states that:

$$||\hat{x}||_\infty \leq 2 - ||f(k)||_1 \tag{10.10}$$

This is a worst case criterion relating the amplitude of the peak input signal to the one based norm of the impulse response of the filter $F(z)$ [43].

This rather conservative criterion can be improved by using the fact that the modulator is invariant to scaling of the feedback filter $H(z)$. This leads to this improved BIBO criterion

$$||\hat{x}||_\infty \leq 3 - S_{min} \tag{10.11}$$

where S_{min} is the global minimum of $S(K_n)$, which is the one based norm of the impulse response of the noise transfer function i.e. [43]

$$S(K_n) = \sum_{i=0}^{\infty} |\mathrm{ntf}_{K_n}(i)| \tag{10.12}$$

When the one based norm of $f(k)$ in (10.10) is below two, the maximum magnitude of the frequency response of the filter $F(z)$ is also bounded by two. This can now be stated as another stability criterion

$$F_{max} = ||F_{min}(z)||_\infty \leq 2 \tag{10.13}$$

where $F_{min}(z)$ is the frequency response of the filter $F(z)$ with a quantizer gain K_n.

10.5 Design of Modulator filter

The design of our 3rd order modulator is based on a noise transfer function NTF(z) with a 3rd order butterworth highpass characteristics, also we have chosen to design for a MSA of 0.37. Based on these choices we get that the A_{min} value is $A_{min} = 2.4074$ and that the cut-off frequency of the butterworth highpass filter, relative to half the sampling frequency, is $f_b = 0.19$

From the BIBO stability criterion we get that $S_{min} = 3.2284$ @ $k = 1.2819$ and $F_{max} = 1.8670$. Because the S_{min} value is larger than three, the BIBO criterion can not guarantee that the modulator will be stable for zero input.

Based on the above design procedure and stability analysis, we end up with the filter coefficients shown in Table 10.1 (se Fig. 10.9).

Table 10.1: Modulator Coefficients scaled for minimum signal swing without feed-input

a_1	a_2	b_1	b_2	b_3	g_1	g_2	g_3
1.0000	0.0000	1.0000	1.5835	2.2263	0.3333	0.7194	1.0000

Simulations have shown that by choosing $a_2 = b_2$ (se Fig. 10.1) the signal swing at the outputs of the integrators is minimized. The modulator coefficients for a modulator with multiple feed-input is shown in Table 10.2.

Table 10.2: Modulator Coefficients scaled for minimum signal swing with feed-input

a_1	a_2	b_1	b_2	b_3	g_1	g_2	g_3
1.0000	0.8000	1.0000	0.8000	1.0000	0.1684	0.6401	1.0000

In order to estimate the overall signal transfer function $\mathrm{STF}_{K_n}(z)$ we first have to estimate the gain of K_n of the quantizer. Assuming that the modulator, when operating, will tend to minimize the noise power at the input of the quantizer, the quantizer gain can be found as the gain that minimizes the two based norm of the error transfer function [43].

$$\mathrm{ETF}_{K_n}(z) = \frac{U_3(z)}{Q(z)} = \frac{-H(z)}{1 + k_n H(z)} \tag{10.14}$$

Based on this assumption we found the quantizer gain to be $K_n = 1.3405$. Using this gain and the modulator filter that we have designed we get the estimated signal transfer function shown in Fig. 10.4. From this figure we see that when using multiple feed-input for reducing

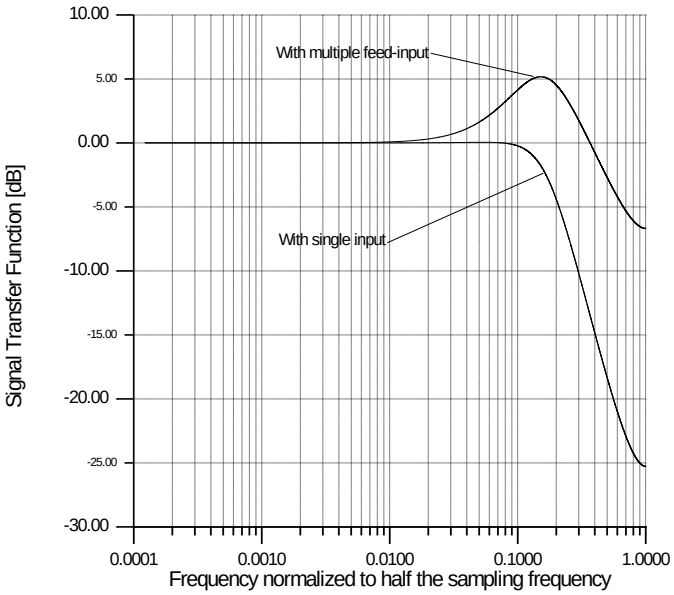

Figure 10.4: Estimated Signal Transfer Function $\mathrm{STF}_{K_n}(z)$

the signal swing at the outputs of the integrators, introduces a significant peak with an amplitude of 5dB. Using an oversampling ratio of $R = 128$, we have that the maximum input signal frequency normalized to half the sampling frequency is given by $1/128 \simeq 0.00781$. At this frequency the peak in the signal transfer function will only introduce a small gain of 0.1dB.

By introducing multiple feed-input to the modulator will have no effect on the noise transfer function, because it is solely determined by the feedback coefficients.

10.5.1 Simulation of the Modulator

All of the simulations performed in this section are done on a behavior level, using a dedicated simulator that I have written in C++.

For each time step the simulator solves all of the nonlinear differential equations involved in the settling of the current copiers, using a 2nd order Runge Kutta Algorithm. This was the only way to simulate the nonlinear settling errors because of the large number of samples required to get reasonably accurate output from the modulator. A transistor level simulation using SPICE would take weeks.

MSA and reliability

In order to determine the exact value of the MSA a simulation was performed using a slow ramp as input signal to the modulator, increasing from 0 to 1 using 100 million iterations. This simulation gave a MSA of MSA = 0.44571.

It is interesting to know whether the modulator is reliable i.e. whether the transition from stable to the unstable region is sharp.

To test the reliability of the modulator, the input range [0;1] is divided into 500 values. For each input value 1000 simulations are performed using random initial conditions for the integrators. Each simulation is performed using maximum 2000 time steps or until the input signal to the comparator exceeds 10, indicating unstability. For each input value (set of 1000 simulations) the longest transient leading to instability within 2000 time steps is recorded. In Fig. 10.5 the longest transient is plotted for each input value.

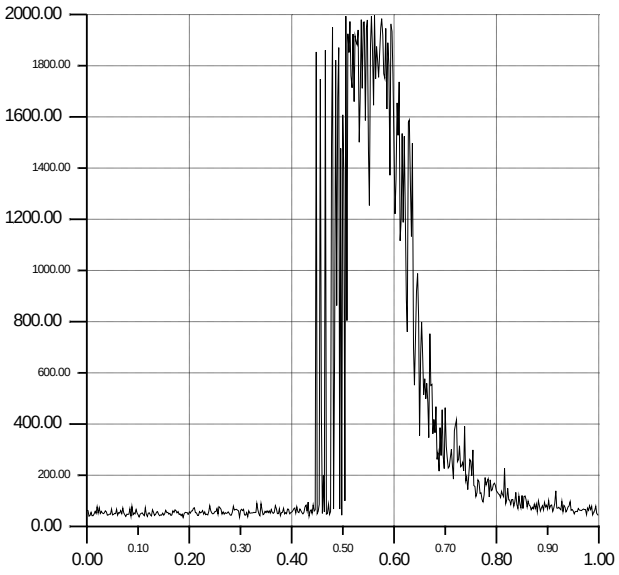

Figure 10.5: Plot of maximum transient length versus constant input

This figure shows that the modulator behaves reliably for input values up to 0.446, this corresponds very well to the result found using a slow ramp. For input values larger that 0.446 the modulator is unreliable seen as the existence of long transients leading to unstability.

Amplitude distribution

In order to illustrate the effect of introducing multiple feed-input for reducing the signal swings at the outputs of the integrators we have performed two simulations, one with and one without the multiple feed-input arrangement.

Both simulations were performed with an input sine wave with an amplitude of 0.43, close to MSA. In Fig. 10.6 we have the amplitude distribution at the outputs of the integrators for the modulator without the multiple feed-input and in Fig. 10.7 we have the amplitude distribution at the outputs of the integrators for the modulator with the multiple feed-input. From these figures it is obvious that by introducing the multiple feed-input the signal swing at the output of the integrators is reduced by approximately a factor of two.

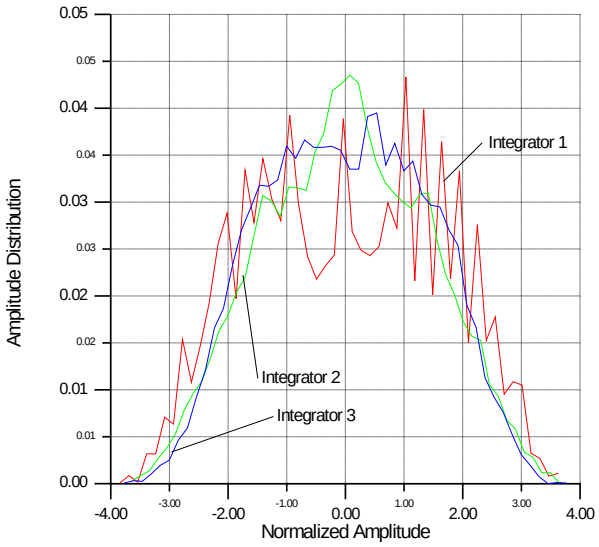

Figure 10.6: Amplitude distribution at the output of the integrators for an input signal of 0.43 and without multiple feed-input

Modulator Spectrum with and without Nonlinear Settling

The current copiers used in the integrators are build from CMOS differential pairs as shown in Fig. 10.11 and Fig. 10.12. This makes the settling behavior nonlinear and signal dependent, see Chapter 4.

Two simulations have been performed; one without settling errors and one with small signal settling errors of 0.5% and with a MOS differential pair as a transconductor. All simulation results are based upon averages of 8 simulation runs, each consisting of 16384 samples. The resulting modulator output spectrum is shown in Fig. 10.8.

The effect of the nonlinear settling errors, caused by the CMOS differential pairs, is an increase in the noise floor at low frequencies, which limits the SNR to 85.9dB as shown in Fig. 10.8. The level of this noise floor is dependent upon the amplitude of the input signal i.e. this noise floor will decrease if we decrease the amplitude of the input signal.

Several simulations were performed for different small signal settling errors and the resulting SNR is shown in Table 10.3. From this table we see that with no settling errors i.e. an ideal modulator the peak SNR is 106.7dB which corresponds to 17.8-Bit's. We also notice

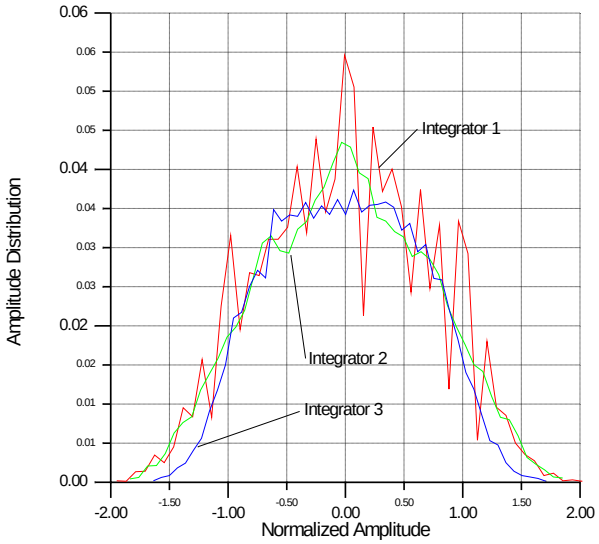

Figure 10.7: Amplitude distribution at the output of the integrators for an input signal of 0.43 and with multiple feed-input

Table 10.3: Relationship between small signal settling error ϵ and resulting SNR

ϵ [%]	SNR [dB]
0	106.7
0.015625	97.2
0.03125	95.4
0.0625	91.5
0.125	89.2
0.25	86.7
0.5	85.9
0.023	96.0

that in order to get a peak SNR of 96dB, the small signal settling error should be made smaller than 0.023%.

10.6 Implementation

To reduce the low frequency $1/f$ noise a special arrangement has been used for the feed forward and feedback branches as shown in Fig. 10.9. The transconductors generating the input currents to the integrators are always connected to the integrators. The effect of this is that the integrators will perform correlated double sampling (CDS) on the noise from the transconductors, which in effect cancels most of the $1/f$ noise.

The choice of saturation voltages for the circuit elements in the sigma-delta modulator are based upon an constrained minimization of the current consumption with regard to a given SNR and supply voltage.

The minimization was performed using the function `CONSTR` in the optimization toolbox in

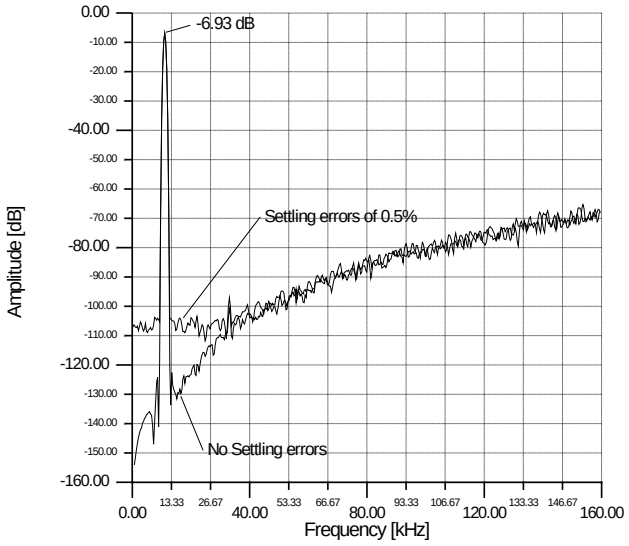

Figure 10.8: Modulator output spectrum with a relative input amplitude of 0.45 (MSA), without settling errors and with settling errors of 0.5%

MATLAB. The optimization methology used, is the same as the one described in Chapter 5.

To show how different choice of supply voltage influences the storage capacitor, current consumption and power consumption for the first integrator in the sigma delta-modulator, some optimizations have been performed, se Table 10.4.

The capacitor values shown in Table 10.4 are sized for a SNR of 96dB. When I design this modulator I had a bug in my simulation program that unfortunately gave results indicating that a settling error of 0.5% should be adequate for a SNR of 96dB. This is however not true as we have seen. In order to get a SNR of 96dB the settling error should be as small as 0.023%. In order to obtain this the bias current $I \cdot N/m_i$ should be increased from $3.7mA$ to $5.9mA$ i.e. by 58%.

Table 10.4: Data for one of the transconductors used in the first integrator, for different choices of V_{DD}. Parameters in the optimization:Relative input amplitude = 0.5, Settling error = 0.5%, Modulation Index $m_i = 0.77$

$V_{DD}[V]$	$C[pF]$	$I \cdot N/m_i[mA]$	$P = V_{DD} \cdot I \cdot N/m_i[mW]$	Dynamic Range [N]
5.00	144.98	8.56	42.82	2
6.00	84.86	6.66	39.98	2
7.00	55.70	5.49	38.45	2
8.00	39.56	4.71	37.69	2
9.00	29.42	4.11	37.01	2
10.00	22.90	3.70	36.96	2
10.00	33.34	10.99	109.93	4

From Table 10.4 we see that lowering the supply voltage has almost no effect on the power consumption, this is due to the folded cascode topology (see Chapter 5). The storage capacitance will however increase drastically when we lower the supply voltage. Therefore

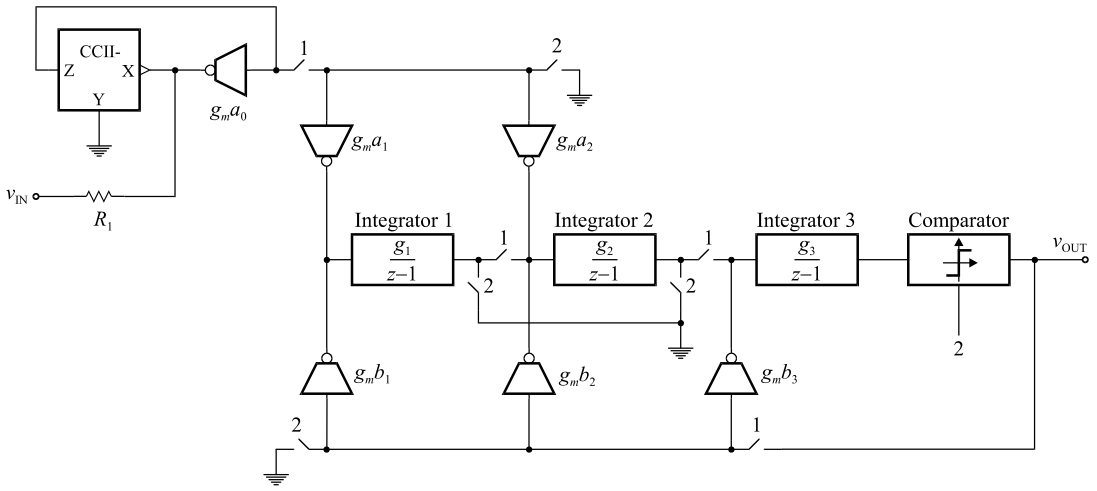

Figure 10.9: Block diagram of the Sigma-Delta Modulator

I chose a supply voltage of $10V$ to get reasonable capacitors sizes. Based on this choice of supply voltage the saturation voltages are found to be the ones shown in Table 10.5.

Table 10.5: Saturation voltages used in the SI circuits i.e. Integrators and Biasing circuitry

$\Delta v_{B1}[V]$	$\Delta v_{B2}[V]$	$\Delta v_{B3}[V]$	$\Delta v_{B4}[V]$	$\Delta v_{B5}[V]$	$\Delta v_s[V]$
3.0	0.5	0.5	3.5	1.7	2.4

Because of the large saturation voltages used in the circuits, there were severe problems with the effect of mobility reduction that had to be taken into account.

10.6.1 Input section and Feed-Input

The input section of the sigma delta modulator consists of a second generation current conveyor CCII− and the transconductors a_0, a_1 and a_2, as shown in Fig. 10.9.

To get a highly linear conversion from the input signal (Voltage) to an internal signal (Current) an internal polysilicon resistor is used, se Fig. 10.9. The resistor is internally connected to a very low impedance node made from a feedback connection of a second generation current conveyor CCII− and a transconductor a_0.

In Fig. 10.10 we have the actual implementation of the input section. All the circuit elements are fully differential in order to get as high performance as possible. The transconductors are basically build from common differential pairs and the CCII− is a foldet cascode structure with a commonmode regulation.

10.6.2 Integrators and Feedback DAC's

The basic SI integrator is build from two fully differential transconductors and a fully differential second generation current conveyor CCII− (see Chapter 2), as shown in Fig. 10.10 and Fig. 10.11.

The two differential transconductors OTA1 and OTA2 are used as current copiers and the CCII− is used to cascode the two differential pairs in order to reduce the current transmission

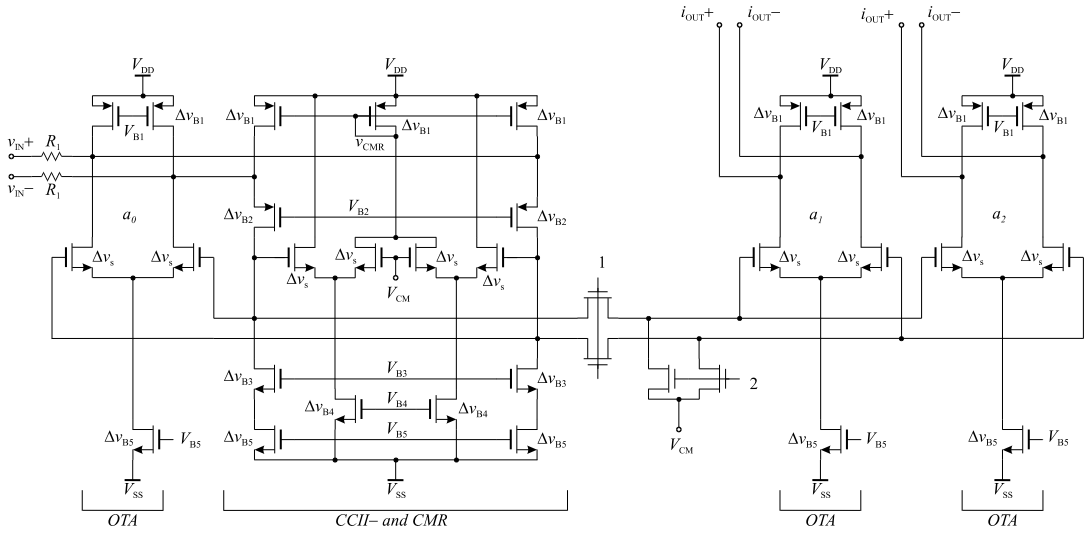

Figure 10.10: Block diagram of the Input section and Feed-Input

errors, when the current is moved from the one current copier to the another. The CCII– is also used for common mode regulation.

The dominating sources of noise and other errors in the modulator is the input section, the first DAC and the first integrator. Any other error sources will be noise shaped by the modulator which will tend to reduce the error.

In Fig. 10.3, integrators 1 and 2 are different from integrator 3 in the sense that integrators 1 and 2 both have an output transconductor OTA3 as shown in Fig. 10.10. Integrator 3 does not have this output transconductor because the comparator looks directly at the differential voltage at the second transconductor OTA2.

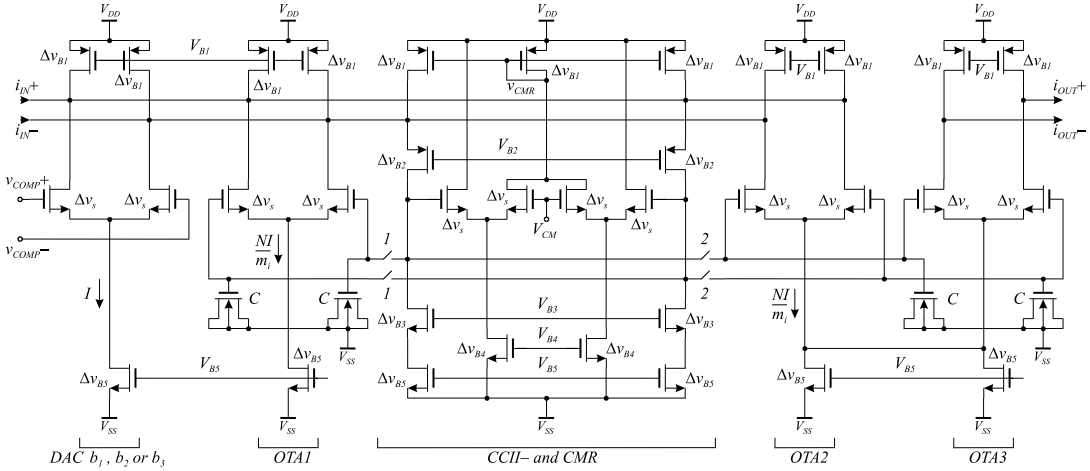

Figure 10.11: Block diagram of the 1st and the 2nd integrator

In Fig. 10.3 the feedback DAC's are shown as transconductors a_1, a_2 and a_3. The actual implementation of one of the DAC's can be seen in Fig. 10.11. It consists basically of a single differential pair used as a current switch.

Because the DAC's are always connected to the input of the integrators they will be

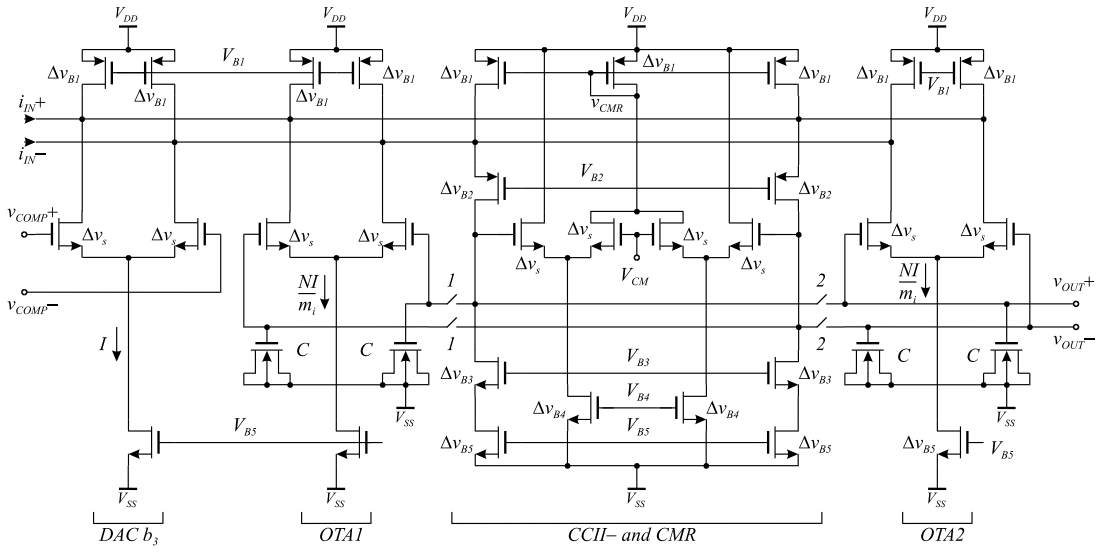

Figure 10.12: Block diagram of the 3rd integrator

exposed to correlated double sampling (CDS) which will tend to cancel the low frequency $1/f$ noise.

10.6.3 Comparator

The comparator used in this design is a fully differential voltage comparator. Using a positive feedback scheme to get a very fast response time [11].

The comparator actually looks at the sign of the differential voltage at the input of the second transconductor in integrator 3.

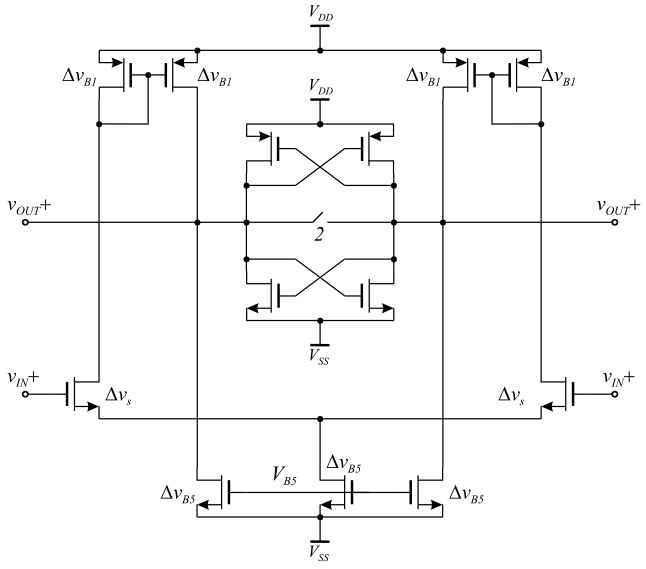

Figure 10.13: Block diagram of the comparator

10.7 Layout

A test chip was implemented in an industry standard analog $2.4\mu m$ CMOS process (MIETEC). All of the Analog and the Digital building blocks were fully custom designed using the Layout editor L-Edit from Tanner Research.

A layout of the whole Sigma-Delta Modulator is shown in Fig. 10.14. This layout shows the main sections of the chip: In the upper left corner we have the non-overlapping clock generator. The clock signals are distributed through a clock bus, shown at the top of the chip, and feed to the switches that control the operation of the integrators and the comparator. In the middle of the chip we have three large sections making up the three integrator INT1, INT2 and INT3. In the lower left corner we have the input section and in the lower right corner we have the comparator. The biasing circuitry is located in between the input section and the comparator.

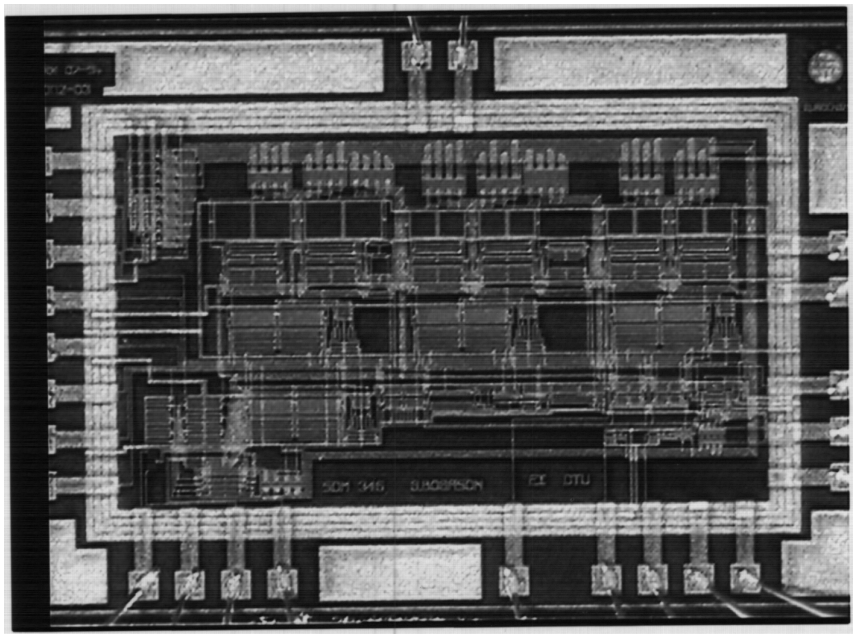

Figure 10.14: Layout of the 3rd order Sigma-Delta Modulator

10.8 Experimental Results

Testing of the fabricated Sigma-Delta modulator showed that it did not operate correctly.

Measurements of the supply current showed that some sort of latchup effect could easily be triggered by varying the supply voltage in a suitable manner. The reason for this could be the lack of substrate contacts around the rather large storage capacitors in the first integrator $180\mu m \times 180\mu m$.

Top level simulation was performed, but only for few clock cycles. This was due to the long simulation time.

Layer-versus-schematic (LVS) check was not completed in the layout phase of the project, therefore it is possible that there are some undetected layout errors on the chip.

The reason for chip not operating correctly was newer fully discovered.

10.9 Conclusion and Future Work

This paper has described the implementation of a 3rd order sigma delta modulator in switched current technique. The choice of modulator structure and implementation details are discussed.

The main limiting factors in the design of high performance $\Sigma - \Delta$ Modulators are the linearity of the Voltage to Current ($V \rightarrow I$) transformation and the high power consumption needed for large Signal-To-Noise-Ratios.

In Chapter 9 we showed that each time we increase the SNR by 6dB i.e. by one bit, we have to increase the power consumption by a factor of four. Also high SNR requires small settling errors that can only be achieved by using large bias currents or linearized transconductors.

In order to cope with these problems a study of linear transconductors and of highly linear Voltage to Current ($V \rightarrow I$) circuits is necessary. Also for A/D Modulators with large dynamic range it might be advantageous to use some sort of floating point scheme i.e. have some sort of automatic scaling of the signals at the input of the modulator.