Chapter 11

Conclusions

In this thesis we have mainly focused on SI circuits. We have shown that circuits performing linear signal processing operations can be built from nonlinear components. This applies to both SI and SC circuits, effectively making SC circuits compatible with digital CMOS processes as well as SI circuits. We have shown that linear signal processing using nonlinear components relies on careful matching of the nonlinearities found in the components.

By treating the SI circuits on a high level using transconductor and current conveyors, we are able to show how many of the already well known current copier cells, and some new ones, can systematically be derived. Based on this high level treatment of current copiers, we are also able to elegantly derive many already known SI building blocks and some new ones. This is done by sharing current conveyors and reducing switches.

It is my hope, that this approach gives a clearer and more fundamental understanding of the operation of the SI circuits.

Simulations have been performed, that confirm the theoretical prediction of the increase of the THD with the signal frequency. These simulation have shown that when using asymmetrical transconductors in the current copiers, it is advantageous to have a equal number of CCOP's in the signal path, because this has the effect of canceling a lot of the even order distortion caused by the settling errors etc. We have also shown that in terms of power consumption, it is more economical to increase the bias current than to decrease the modulation index, in order to reduce any settling errors.

From noise analysis of SI circuits we have shown that there exists an optimal choice of saturation voltages and modulation index, that minimizes the power consumption, the storage capacitance etc. We have also shown that using constrained optimization, these saturation voltages and modulation index can be found.

We have shown that the SNR depends only on the choice of saturation voltages and modulation index, it does not directly depend on the bias current. The bias current is determined by the settling errors and the operating speed of the circuitry.

We have shown that using the switched current technique it is possible to design 4th order lowpass and highpass filters, with good tracking between the cut-off frequencies of the highpass and lowpass filter sections, using relatively simple circuit configurations. Operation with supply voltages down to $2V$ is possible with a power consumption of $200\mu W$.

In order to avoid severe stability and settling problems we have shown that SI filters should be based on building blocks that do contain at least one sample delay between input and output. Therefore it is not a good idea to use differentiators and bilinear integrators as basic filter building blocks, because it can lead to high power consumption and low SNR. SI filters should preferably be based on sample delay integrators.

We have shown that it is feasible to implement a multiplierless adaptive filter with 96 filter taps in switched current technique, with small power consumption and reasonable chip area. A chip containing 96 filter taps occupies an area of $3.8mm \times 3.8mm$ and contains approximately 9500 MOS transistors.

We have shown that a low cost serial A/D and D/A system can be build using relatively simple SI building blocks, and implemented fully in a digital CMOS process. By combining successive approximation with a serial conversion scheme we are able to produce a A/D and D/A converter that reuses the same hardware in both A/D and D/A mode of operation.

Operation with supply voltages down to $2.3V$ is possible with a current consumption of $38.5\mu A$.

For Sigma-Delta modulators implemented in SI technique we have shown, that for a given SNR, the power consumption is independent of the oversampling ratio R, and depends only on the required SNR. We have also shown that each time we increase the SNR by 6dB we have to increase the power consumption by a factor of four. Therefore a large SNR is very expensive in terms of power consumption.

The main limiting factors in the design of high performance $\Sigma\Delta$ Modulators is the linearity of the Voltage to Current ($V \rightarrow I$) transformation and the high power consumption needed for large Signal-To-Noise-Ratios. Also high SNR requires small settling errors that only can be achieved by using large bias currents or linearized transconductors.

In order to cope with these problems a study of linear transconductors and of highly linear Voltage to Current ($V \rightarrow I$) circuits is necessary. Also for A/D Modulators with large dynamic range it might be advantageous to use some sort of floating point scheme i.e. have some sort of automatic scaling of the signals at the input of the modulator.

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Part III

Appendix

Appendix A

MOS Transconductors

This appendix introduces many of the most common transconcuctors, and tries to describe many of their most important properties. In this description of the most common transconductors we will only consider transconductors using MOS transistors operating in strong inversion and saturation.

The description of the transconductors is deliberately done using the saturation voltage $\Delta v = (v_{GS} - V_T)$ as a key parameter. The saturation voltage for a MOS transistor is the minimum drain-source voltage that is required in order to keep the transistor in its saturated region.

The reason for focusing on the saturation voltage is that it is a very useful design parameter when designing SI circuits. This is mainly because it allows for easy calculation of the necessary voltage drops in the SI circuits.

A somewhat similar description of various transconductors is given in [25], but this description does not focus on the saturation voltage Δv as a key design parameter.

A.1 The MOS Transistor

The simplest MOS transconductor that we have is the single MOS transistor shown in Fig. A.1. The description of this transconductor will be done using the simple Schiman and Hodges model (SPICE Level one). This is mainly done because this model allows for easy hand calculations of the transistor parameters. The basic and most important relation-

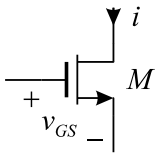

Figure A.1: A single MOS transistor

ships for this transistor is the relationship between the drain current i and the gate-source voltage v_{GS}, we have that

$$i = \frac{\beta}{2}\left(v_{GS} - V_T\right)^2 \ , \ v_{DS} > (v_{GS} - V_T) = \Delta v \tag{A.1}$$

From this equation we can now find the gate-source voltage as a function of the threshold voltage V_T and the saturation voltage Δv

$$v_{GS} = V_T + \sqrt{\frac{2i}{\beta}} = V_T + \Delta v \tag{A.2}$$

The transconductance is found as the derivative of the drain current with respect to the gate-source voltage v_{GS}

$$g_m = \frac{\partial i}{\partial v_{GS}} = \beta\left(v_{GS} - V_T\right) = \frac{2i}{\Delta v} \tag{A.3}$$

A.2 The Compound MOS Transistor

A compound MOS transistor is a combination of a single NMOS transistor and a single PMOS transistor as shown in Fig. A.2. We will show that the compound MOS transistor is equivalent to a single MOS transistor, with an effective gate-source voltage given by the voltage drop $v_1 - v_2$ and a threshold voltage equal to the sum of the threshold voltages of the individual MOS transistors. An equation describing the effective gate-source voltage $v_1 - v_2$

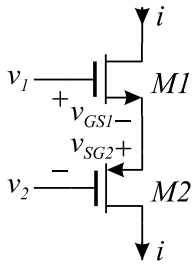

Figure A.2: A compound MOS transistor

is given by

$$\begin{aligned} v_1 - v_2 &= v_{GS1} + v_{SG2} && \text{(A.4)} \\ &= (V_{T1} + V_{T2}) + \sqrt{\frac{2i}{\beta_1}} + \sqrt{\frac{2i}{\beta_2}} = (V_{T1} + V_{T2}) + (\Delta v_1 + \Delta v_2) && \text{(A.5)} \\ &= (V_{T1} + V_{T2}) + \sqrt{2i}\left(\frac{1}{\sqrt{\beta_1}} + \frac{1}{\sqrt{\beta_2}}\right) && \text{(A.6)} \end{aligned}$$

this equation can be written as

$$v_1 - v_2 = (V_{T1} + V_{T2}) + \sqrt{\frac{2i}{\beta}} \text{ , where } \beta = \frac{\beta_1\beta_2}{\left(\sqrt{\beta_1} + \sqrt{\beta_2}\right)^2} \tag{A.7}$$

From the above equation we can now find the relationship between the drain current i and the effective gate-source voltage $v_1 - v_2$.

$$i = \frac{\beta}{2}\left((v_1 - v_2) - (V_{T1} + V_{T2})\right)^2 \tag{A.8}$$

The above equation shows that a compound MOS transistor operates as a single MOS transistor with a threshold voltage equal to the sum of the two threshold voltages and with an effective gate-source voltage determined by the voltage difference between the gates $v_1 - v_2$.

The transconductance of the compound MOS transconductor can be found using (A.3)

$$g_m = \frac{2i}{\Delta v_1 + \Delta v_2} \tag{A.9}$$

A.3 The MOS Differential pair

One of the most important and most widely used transconductors is the MOS differential pair shown in Fig. A.3. For this differential pair we will derive some very important equations describing the relationship between the differential output current $i_D = i_1 - i_2$, as a function of the input differential voltage $v_D = v_1 - v_2$. We will also derive the relationship between the differential transconductance g_m and the differential voltage. And at last we will show a relationship between the source voltage v_S and the voltage v_1 and v_2. For the differential

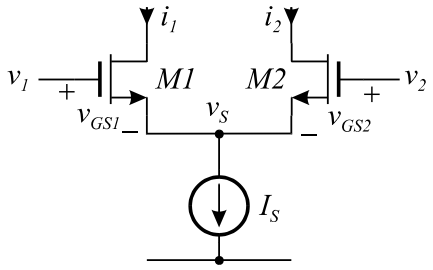

Figure A.3: MOS Differential pair

pair we have that the sum of the two drain currents is given by

$$i_1 + i_2 = I_S \tag{A.10}$$

and the saturation voltage of the two transistors M1 and M2 is given by

$$\Delta v_1 = \Delta v_2 = \Delta v_S = \sqrt{\frac{I_S}{\beta}} \tag{A.11}$$

A.3.1 Relationship between output current and differential voltage

From Fig. A.3 we have that the differential voltage v_D is given by

$$v_D = v_1 - v_2 = v_{GS1} - v_{GS2} \tag{A.12}$$

assuming that the two transistors M1 and M2 have the same threshold voltages we get that

$$v_D = \sqrt{\frac{2i_1}{\beta}} - \sqrt{\frac{2i_2}{\beta}} \tag{A.13}$$

$$\Downarrow \tag{A.14}$$

$$v_D^2 = \frac{2i_1}{\beta} + \frac{2i_2}{\beta} - 2\sqrt{\frac{4i_1 i_2}{\beta^2}} \tag{A.15}$$

$$= \frac{2}{\beta} I_S - \frac{4}{\beta}\sqrt{i_1 i_2} \tag{A.16}$$

from the above equation we get that the product of the two drain currents i_1 and i_2 is given by

$$i_1 \cdot i_2 = \left(\frac{I_S}{2} - \frac{\beta}{4}v_D^2\right)^2 \tag{A.17}$$

If we apply a large differential voltage v_D at the differential pair, one of the transistors M1 or M2 will be cut off and the current in the second transistor will saturate at I_S. Therefore the product of the two drain currents at the maximum differential voltage $v_{D,max}$ will be zero. Using this fact we can find the maximum differential voltage from (A.17)

$$\frac{I_S}{2} - \frac{\beta}{4}v_{D,max}^2 = 0 \tag{A.18}$$

which gives

$$v_{D,max}^2 = \frac{2I_S}{\beta} \tag{A.19}$$

$$\Downarrow$$

$$v_{D,max} = \sqrt{2}\sqrt{\frac{I_S}{\beta}} = \sqrt{2}\Delta v_S \tag{A.20}$$

This equation shows that the maximum differential voltage $v_{D,max}$, i.e. the differential voltage that saturates the differential pair, is $\sqrt{2}$ higher than the saturation voltage Δv_S of the transistors used in the differential pair.

If we multiply (A.10) with i_1 and combine that result with (A.17) we get the following equations

$$i_1^2 + i_1 \cdot i_2 = i_1 \cdot I_S \tag{A.21}$$

$$\Downarrow$$

$$i_1^2 + \left(\frac{I_S}{2} - \frac{\beta}{4}v_D^2\right)^2 - i_1 \cdot I_S = 0 \tag{A.22}$$

This is a simple quadratic equation and the solution is easily found as

$$i_1 = \frac{I_S + \sqrt{I_S^2 - 4\left(\frac{I_S}{2} - \frac{\beta}{4}v_D^2\right)^2}}{2} \tag{A.23}$$

$$= \frac{I_S}{2} + v_D\frac{\sqrt{I_S\beta}}{2}\sqrt{1 - \frac{\beta}{4I_S}v_D^2} \tag{A.24}$$

By combining the above equation with (A.10) and (A.20) we get that the two drain currents i_1 and i_2 can be written as

$$i_1 = \frac{I_S}{2} + \frac{v_D}{v_{D,max}}\frac{I_S}{\sqrt{2}}\sqrt{1 - 0.5\left(\frac{v_D}{v_{D,max}}\right)^2} \tag{A.25}$$

and

$$i_2 = \frac{I_S}{2} - \frac{v_D}{v_{D,max}}\frac{I_S}{\sqrt{2}}\sqrt{1 - 0.5\left(\frac{v_D}{v_{D,max}}\right)^2} \tag{A.26}$$

From the two above equations we get that the differential output current i_D is given by

$$i_D = i_1 - i_2 = \frac{v_D}{v_{D,max}}I_S\sqrt{2}\sqrt{1 - 0.5\left(\frac{v_D}{v_{D,max}}\right)^2} \tag{A.27}$$

In Fig. A.4 we have plotted (A.27).

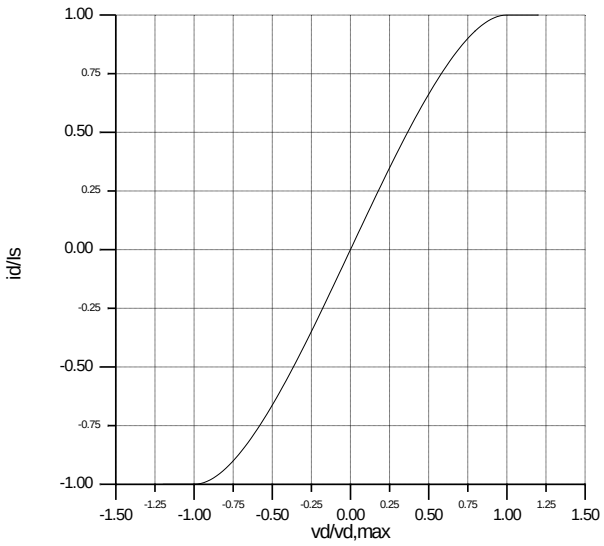

Figure A.4: Relationship between differential output current and differential input voltage for a MOS differential pair

A.3.2 Relationship between transconductance and differential voltage

The voltage dependent transconductance of the differential pair can be found as the derivative of (A.27).

$$\frac{\partial i_D}{\partial v_D} = g_m(v_D) = g_{m0}\frac{1-\left(\frac{v_D}{v_{D,max}}\right)^2}{\sqrt{1-\left(\frac{v_D}{v_{D,max}}\right)^2}} \text{ , where } g_{m0} = \frac{I_S}{\Delta v_S} \tag{A.28}$$

In Fig. A.5 we have plotted (A.28).

A.3.3 Relationship between source voltage v_S and the voltages v_1 and v_2

When we apply a differential voltage to the differential pair shown in Fig. A.2, the voltage v_S at the source of M1 and M2 increases. A equation describing the relationship between the voltage v_S an the applied voltages v_1 and v_2 can be found by noting that

$$v_S = v_1 - v_{GS1} \tag{A.29}$$

$$v_S = v_2 - v_{GS2} \tag{A.30}$$

which gives us the following relationship

$$v_S = \frac{v_1+v_2}{2} - \frac{v_{GS1}+v_{GS2}}{2} \tag{A.31}$$

From (A.25) and (A.26) we can derive the voltages v_{GS1} and v_{GS2} which when inserted into the above equation, gives

$$v_S = \frac{v_1+v_2}{2} - V_T - \Delta v \cdot f(\frac{v_D}{v_{D,max}}) \tag{A.32}$$

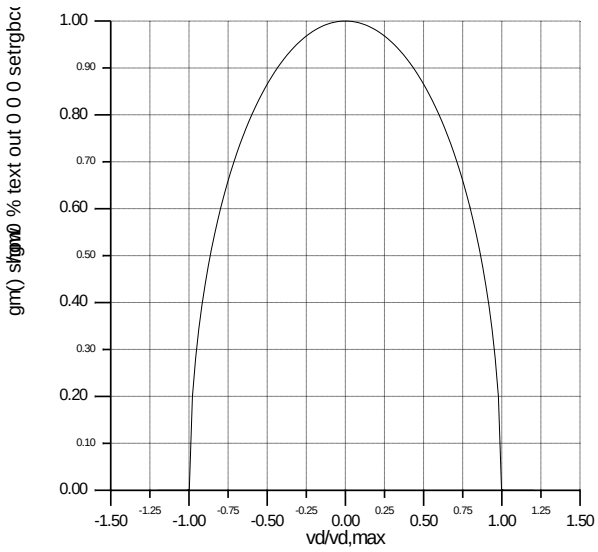

Figure A.5: Relationship between transconductance and differential input voltage for a MOS differential pair

where the function $f(\cdot)$ is given by

$$f(x) = \frac{\sqrt{1+\sqrt{2}x\sqrt{1-0.5x^2}}+\sqrt{1-\sqrt{2}x\sqrt{1-0.5x^2}}}{2} \quad \text{(A.33)}$$

$$= \frac{\sqrt{1+\sqrt{1-x^2(2-x^2)}}}{\sqrt{2}} \quad \text{(A.34)}$$

$$\simeq 1-0.285x^2 \ , \ x \in [-1;+1] \quad \text{(A.35)}$$

This function is plotted in Fig. A.6.

A.4 Resistor Degenerated Differential pair

Very often a MOS differential pair is linearized using resistor degeneration, as shown in Fig. A.7. The two resistors in the differential pair in Fig. A.7 will have a local feedback effect on the transistors M1 and M2, reducing the small signal transconductance and increasing the input voltage range. The small signal transconductance with the two resistors is given by

$$g_m = \frac{g_{m0}}{1+g_{m0}R_S} \quad \text{(A.36)}$$

where g_{m0} is the transconductance without resistor degeneration, which is given by

$$g_{m0} = \frac{I_S}{\Delta v_S} \quad \text{(A.37)}$$

The voltage drop v_{R_S} across the resistors R_S is given by

$$v_{R_S} = R_S\frac{I_S}{2} \quad \text{(A.38)}$$

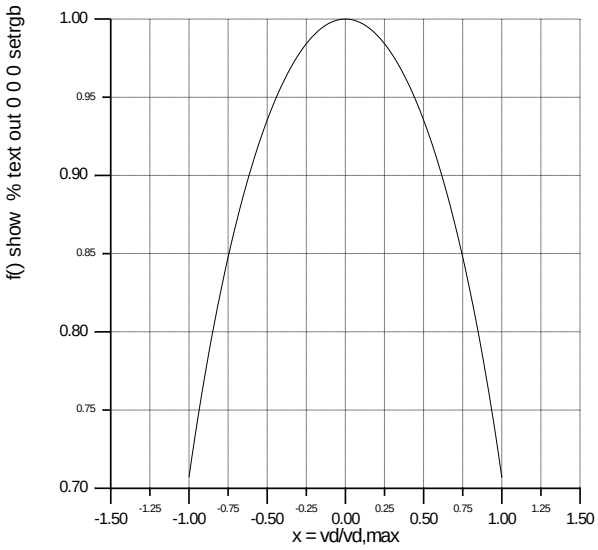

Figure A.6: Plot of the function $f(x)$

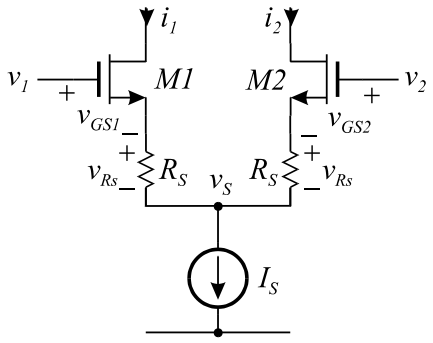

Figure A.7: A MOS differential pair degenerated with two resistors

By combining (A.36), (A.37) and (A.38) we get that the small signal transconductance can be written as

$$g_m = \frac{g_{m0}}{1 + 2\frac{v_{R_S}}{\Delta v_S}} \tag{A.39}$$

So the linear input voltage range has been increased from

$$v_{lin,0} = \frac{I_S}{g_{m0}} = \Delta v_S \tag{A.40}$$

to

$$v_{lin,R_S} = \frac{I_S}{g_m} = I_S \frac{1 + 2\frac{v_{R_S}}{\Delta v_S}}{g_{m0}} = \Delta v_S + 2v_{R_S} \tag{A.41}$$

The above equations show that by using resistor degeneration, the input voltage range of the MOS differential pair is increased by two times the voltage drop v_{R_S} across the source resistors R_S.

A.5 Linear MOS Transconductors

In some applications it is desirable to have a transconductor with a linear relationship between the input voltage and the output current. None of the previously described transconductors have that property. A linear transconductor can be build from MOS transistors by reliing on their square-law relationship between the gate-source voltage and their drain current, see (A.1).

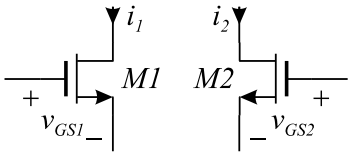

Figure A.8: MOS transistors used in a linear transconductor

Assuming that the two transistors M1 and M2 in Fig. A.8 have the same threshold voltage V_T and the same β, we get that the two drain currents i_1 and i_2 can be written as

$$i_1 = \frac{\beta}{2}(v_{GS1} - V_T)^2 = \frac{\beta}{2}\left(v_{GS1}^2 + V_T^2 - 2V_T v_{GS1}\right)^2 \quad (A.42)$$

$$i_2 = \frac{\beta}{2}(v_{GS2} - V_T)^2 = \frac{\beta}{2}\left(v_{GS2}^2 + V_T^2 - 2V_T v_{GS2}\right)^2 \quad (A.43)$$

By subtracting the two currents above, we get that the differential output current is given by

$$\begin{aligned} i_D &= i_1 - i_2 = \frac{\beta}{2}\left(v_{GS1}^2 - v_{GS2}^2 - 2V_T(v_{GS1} - v_{GS2})\right) \\ &= \frac{\beta}{2}\left((v_{GS1} + v_{GS2}) - 2V_T\right)(v_{GS1} - v_{GS2}) \end{aligned} \quad (A.44)$$

This equation shows that it is possible to get a linear transconductor from the two transistors shown in Fig. A.8 if are able to ensure that $(v_{GS1} - v_{GS2})$ is proportional to the input voltage and that $(v_{GS1} + v_{GS2})$ is constant and equal to twice some commonmode voltage i.e

$$v_{GS1} - v_{GS1} = v_D \quad (A.45)$$

$$v_{GS1} + v_{GS1} = 2V_C \quad (A.46)$$

By rearranging the above equations we get that the gate-source voltages are given by

$$v_{GS1} = V_C + \frac{v_D}{2} \quad (A.47)$$

$$v_{GS2} = V_C - \frac{v_D}{2} \quad (A.48)$$

These equations show that in order to get a linear differential output current from the two MOS transistors shown in Fig. A.8, we have to make sure that each of the gate-source voltages v_{GS1} and v_{GS2} varies linearly with the input voltage v_D. If we compare the two above equations with Fig. A.8 we notice that the commonmode voltage V_C must be equal to

$$V_C = V_T + \Delta v_S \quad (A.49)$$

Assuming that we have satisfied the above constraints we get from (A.44) that the differential output current is given by

$$i_D = \beta(V_C - V_T)v_D = g_m v_D \tag{A.50}$$
$$= \beta \Delta v_S v_D \tag{A.51}$$

If we insert (A.47) and (A.48) into (A.42) and (A.43) we get that the two output currents i_1 and i_2 can be written as

$$i_1 = \frac{\beta}{2}\left((V_C - V_T) + \frac{v_D}{2}\right)^2 = \frac{\beta}{2}\left(\Delta v_S + \frac{v_D}{2}\right)^2 \tag{A.52}$$
$$i_2 = \frac{\beta}{2}\left((V_C - V_T) - \frac{v_D}{2}\right)^2 = \frac{\beta}{2}\left(\Delta v_S - \frac{v_D}{2}\right)^2 \tag{A.53}$$

These equations show that each of the output currents i_1 and i_2 will have a square-law relationship with the input differential voltage v_D, and that the difference i_D between the output currents i_1 and i_2 will be linear as expected. The linear relationship only holds as long as both of the output current are not zero. Based on this we find the minimum and maximum differential input voltage to be

$$v_{D,min} = -2\Delta v_S \tag{A.54}$$
$$v_{D,max} = +2\Delta v_S \tag{A.55}$$

Also we have that the sum of the drain currents i_1 and i_2 is given by

$$i_1 + i_2 = \beta \Delta v_S^2 + \frac{\beta}{4} v_D^2 \tag{A.56}$$
$$= \frac{g_m^2}{\beta} + \frac{\beta}{4} v_D^2 \tag{A.57}$$

which shows that the sum of the output currents consists of a constant term plus a term that varies with the square of the input differential voltage. The constant term is equal to twice the quiescent current in each of the transistors M1 and M2 shown in Fig. A.8. Therefore the quiescent current in each of the transistors M1 and M2 is given by

$$\frac{I_S}{2} = \frac{\beta}{2}\Delta v_S^2 \tag{A.58}$$

If we insert (A.55) into (A.51) we get that the maximum linear differential output current can be found to be

$$i_{D,max} = \beta \Delta v_S 2\Delta v_S = 2\beta \Delta v_S^2 \tag{A.59}$$

which is four times the quiescent current in each of the transistors M1 and M2. The output currents i_1, i_2 and i_D are shown in Fig. A.9

A.5.1 Linearized MOS Differential pair

We have previously described the behavior of a MOS differential pair and found that it has a highly nonlinear relationship between its output current and input voltage, see (A.27). It is however possible to linearize a MOS differential pair using adaptive biasing as we will show now. From (A.24) we get that the differential output current can be written as

$$i_D = v_D \sqrt{\beta I_S - \frac{\beta^2}{4} v_D^2} \tag{A.60}$$

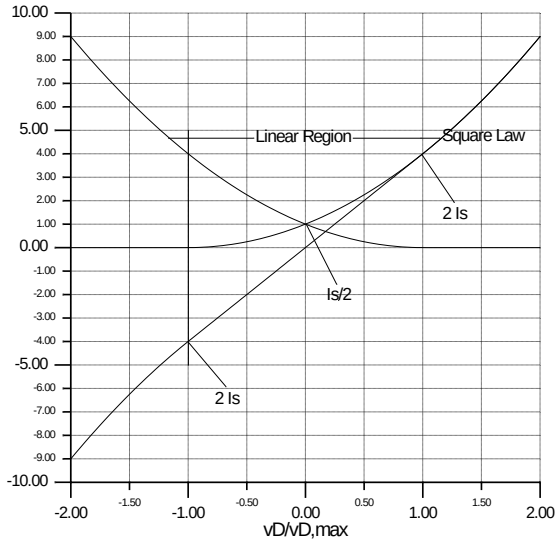

Figure A.9: Plot of the output currents of the linear MOS transconductor

A linear transconductor will have the following relationship between its output current and its input voltage

$$i_D = v_D g_m \tag{A.61}$$

If we compare this equation with (A.60) we see that it might be possible to linearize a MOS differential pair by controlling the tail current I_S in a suitable manner. From (A.60) we see that I_S should be controlled so that the transconductance

$$g_m = \sqrt{\beta I_S - \frac{\beta^2}{4} v_D^2} \tag{A.62}$$

is independent of the differential voltage v_D i.e.

$$I_S = \frac{g_m^2}{\beta} + \frac{\beta}{4} v_D^2 \tag{A.63}$$

This equation is exactly the same as (A.57) which indicates that the adaptive biasing scheme actually performs the linearization by ensuring that the gate-source voltages of the two MOS transistors, that form the differential pair, vary linearly with the input differential voltage.

Appendix B

Current Transmission Errors

When designing useful SI circuits e.g. Filters and A/D converters we have to combine several current copiers and current mirrors in order to design the fundamental building block e.g. integrators, differentiators etc.

The current copier and the current mirror can be thought of as being the most fundamental building block for any SI circuit. It is therefore interesting to identify the errors associated with the interconnection of these basic building blocks [51][26][6][9][20]. To illustrate this we will look at the connection of current mirrors and current copiers. In Fig. B.1 we have a

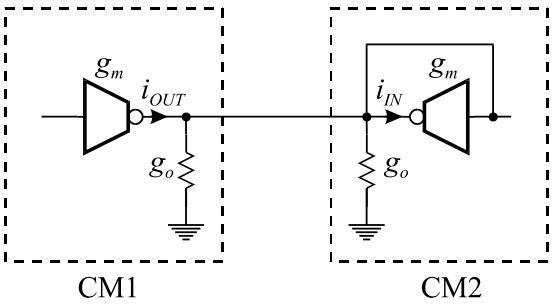

Figure B.1: A current output feeding the input of a current mirror.

situation where we want to transmit the current i_{OUT} from the current mirror CM1 to the input of the transconductor i_{IN} in current mirror CM2. For simplicity we will assume that the all of the transconductors have the same small-signal transconductance g_m and the same small-signal output conductance g_o. It is now easy to realize that the transfer function from i_{OUT} to i_{IN} is given by

$$\frac{i_{IN}}{i_{OUT}} = \frac{g_m}{g_m + 2g_o} = \frac{1}{1 + 2\frac{g_o}{g_m}} \simeq 1 - 2\frac{g_o}{g_m} = 1 - 2\frac{1}{A_i} \tag{B.1}$$

From this equation we see that there will be some current loss determined by the ratio g_m/g_o i.e. by the intrinsic gain of the transconductors. If we e.g.use single MOS transistors as transconductors the intrinsic gain will be limited to about 200 giving a current loss of approximately 1%. For most practical SI circuits this is far to much. From this fact we are led to the conclusion that simple SI circuits based on single MOS transistor transconductors will have a very poor performance.

In Fig. B.2 we have a situation where we want to transmit the current stored in a current copier CCOP1 to the input of an other current copier CCOP2. The current copiers are shown

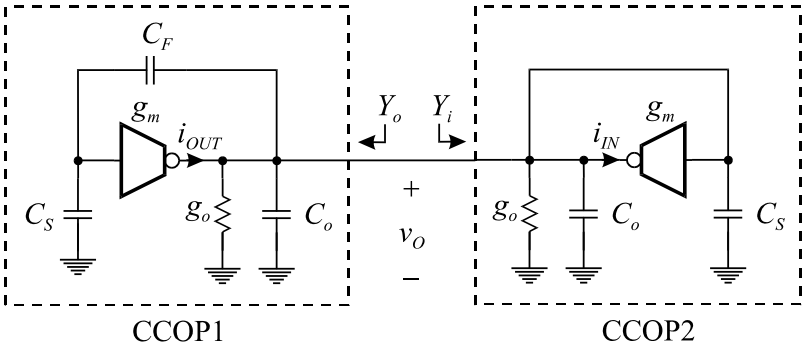

Figure B.2: A current copier in hold mode feeding the input of an other current copier in the copy phase.

with most of their parasitics. From this figure we can identify the following conductance's

$$Y_o = g_o + sC_o + g_m\frac{C_F}{C_S + C_F} \tag{B.2}$$

$$Y_i = g_0 + g_m + s(C_S + C_o) \tag{B.3}$$

we can now calculate the transfer function from i_{OUT} to i_{IN} as being

$$\frac{I_{in}}{I_{out}} = \frac{g_m}{Y_0 + Y_i} = \frac{g_m}{s(C_S + C_o) + g_m + 2g_o + g_m\frac{C_F}{C_S+C_F}} \tag{B.4}$$

We know that the output current i_{OUT} is a sampled and held i.e. a current step. Using this fact we can calculated the current transfer from i_{OUT} to i_{IN} for $t \to \infty$

$$\lim_{s=0} s\frac{1}{s}\frac{I_{in}}{I_{out}} = \frac{g_m}{g_m + 2g_o + g_m\frac{C_F}{C_F+C_S}} = \frac{1}{1 + 2\frac{g_o}{g_m} + \frac{C_F}{C_F+C_S}} \tag{B.5}$$

$$\simeq \underline{1 - 2\frac{g_o}{g_m} - \frac{C_F}{C_F + C_S}} \tag{B.6}$$

This is actually the same result as we found for the current mirror with the exception of an extra term caused by the feedback capacitance C_F.

From the above calculations we observe that in order to decrease the transmission errors it is necessary to decrease g_o/g_m and to decrease C_F/C_S.

Appendix C

Switching Transients

The signals carried around in a switched current circuit are current pulses. These current pulses have a high frequency content and will therefore cause some transients and ringing in the circuit elements [14][15][24][25]. In order to identify the most significant transients we will look at the copy phase and output phase of a current copier. In Fig. C.1 we have a

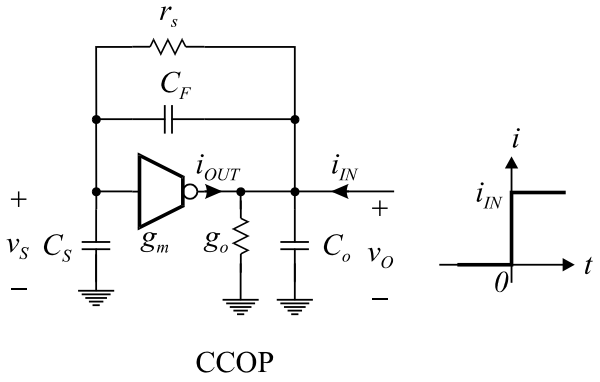

Figure C.1: A current copier in its copy phase.

current copier including all major parasitics even the on-resistance r_s of the feedback switch. We will assume that we are feeding this current copier from an other current copier i.e. the input current will be a step function.

In the ideal case there would be no parasitics C_F, C_o, g_o and the switch on-resistance r_s would be zero. This would lead to a single pole system where $v_S = v_O$. The transfer function from i_{IN} to v_S would be given by

$$\frac{V_S}{I_{in}} = \frac{1}{g_m}\frac{\omega_0}{s+\omega_0} \ , \ \omega_0 = \frac{g_m}{C_S} \tag{C.1}$$

here ω_0 is the bandwidth of the current copier. This simple exponential settling behavior described by the above equation is desirable because it leads to fast settling response.

In most practical SI circuits, the settling behavior is not described by a simple first order system because of the parasitics found in the circuit. By investigating the circuit in Fig. C.1 we see that we have two basic nodes which gives the following node equations

$$\begin{bmatrix} s\left(C_S + C_F\right) + g_s & -\left(sC_F + g_s\right) \\ g_m - \left(sC_F + g_s\right) & s\left(C_F + C_o\right) + g_o + g_s \end{bmatrix} \begin{bmatrix} V_s \\ V_o \end{bmatrix} = \begin{bmatrix} 0 \\ i_{IN} \end{bmatrix} \tag{C.2}$$

from these equations we can derive the following approximate transfer function

$$\frac{V_s}{I_{in}} = \frac{g_s}{s^2 C_S(C_F + C_S) + sC_S g_s + g_m g_s} = \frac{\frac{g_s}{C_S(C_F+C_o)}}{s^2 + s\frac{g_s}{(C_F+C_o)} + \frac{g_m g_s}{C_S(C_F+C_o)}} \tag{C.3}$$

the denominator polynomial in the above transfer function can now be written as

$$\left(s + \frac{g_s}{2(C_F + C_o)}\right)^2 + \frac{4(C_F + C_o)g_m g_s - g_s^2 C_S}{4C_S(C_F + C_o)^2} \tag{C.4}$$

this denominator polynomial determines the stability properties of the circuit, and we can now classify the settling behavior of the current copier in its copy phase, as shown below

- Damped

$$4(C_F + C_o)g_m g_s - g_s^2 C_S < 0 \Leftrightarrow \omega_0 = \frac{g_m}{C_S} < \frac{g_s}{4(C_F + C_o)} \tag{C.5}$$

- Critical damping

$$4(C_F + C_o)g_m g_s - g_s^2 C_S = 0 \Leftrightarrow \omega_0 = \frac{g_m}{C_S} = \frac{g_s}{4(C_F + C_o)} \tag{C.6}$$

- Oscillating

$$4(C_F + C_o)g_m g_s - g_s^2 C_S > 0 \Leftrightarrow \omega_0 = \frac{g_m}{C_S} > \frac{g_s}{4(C_F + C_o)} \tag{C.7}$$

From these equations we see that in order to avoid oscillating settling behavior we have to make sure that the time constant C_S/g_m of the CCOP is not made smaller than four times the time constant made from the switch on-resistance r_s and the parasitic capacitors C_F and C_o.

In high-speed SI circuits one might get into problems with oscillating settling behavior because the bandwidth of the CCOP must be high, i.e. a small time constant, in order to allow for the high operating speed.

In low-noise SI circuits one would have to use a large storage capacitor C_S in order to get low kT/C noise. This implies that low-noise SI circuits will normally experience damped settling behavior dominated by the bandwidth of the current copier. It is however possible to get oscillating settling behavior in low-noise SI circuits, especially if the large storage capacitance C_S is the gate-source capacitance of the transconductor transistor. A large gate-source capacitance requires a wide transistor leading to a large drain-bulk junction capacitance which contributes directly to the output parasitic capacitance. In order to circumvent oscillating settling behavior in low-noise SI circuits it is often advantageous to make a part of the storage capacitance C_S separate from the transconductor transistor e.g. by using a separate MOS capacitor.

In Fig. C.2 we have a situation where the output of current copier CCOP1 is connected to the input of current copier CCOP2. Fig. C.2 is basically derived from Fig. B.2 and will be used to illustrate the transient found at the output of a CCOP when it is connected to the input of an other CCOP.

We will assume that current copier CCOP1 has previously been loaded with some current and that the settling behavior was damped and dominated by the bandwidth of the current copier itself. This implies that the capacitors C_S and C_o have been charged to the same voltage v_{S0}. We will also assume that there is stored no current in current copier CCOP2 when it is connected to current copier CCOP1.

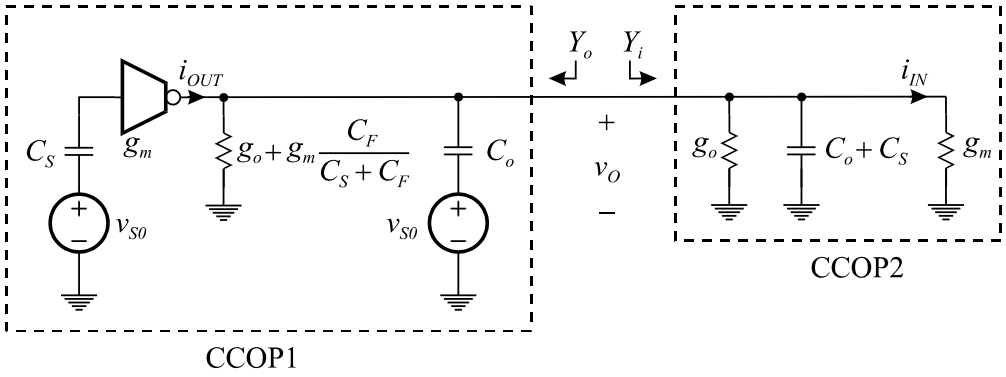

Figure C.2: A current copier in its hold phase while feeding the input of an other current copier.

We have in Chapter B discussed how the transfer function from i_{OUT} to i_{IN} is determined after all transients have died out. Now we will focus on how the transient voltage v_O behaves. From Fig. C.2 we get the following relationship

$$V_o(s) = \frac{\frac{v_{S0}}{s}(sC_o - g_m)}{Y_i + Y_o} = v_{S0}\left(\frac{\frac{C_o}{C_S+2C_o}}{s + \frac{g_m+2g_o+g_m\frac{C_F}{C_S+C_F}}{C_S+2C_o}} - \frac{\frac{g_m}{C_S+2C_o}}{s\left(s + \frac{g_m+2g_o+g_m\frac{C_F}{C_S+C_F}}{C_S+2C_o}\right)}\right) \tag{C.8}$$

the corresponding time function can be found using inverse $\mathcal{L}$aplace transform

$$v_O(t) = v_{S0}\left(\frac{C_o}{C_S+2C_o}e^{-\omega_1 t} - \frac{1-e^{-\omega_1 t}}{1+2\frac{g_o}{g_m}+\frac{C_F}{C_S+C_F}}\right) \tag{C.9}$$

where

$$\omega_1 = \frac{g_m + 2g_o + g_m\frac{C_F}{C_S+C_F}}{C_S+2C_o} \simeq \omega_0 = \frac{g_m}{C_S} \tag{C.10}$$

The transient voltage given by (C.9) has been plotted in Fig. C.3 and we see that the

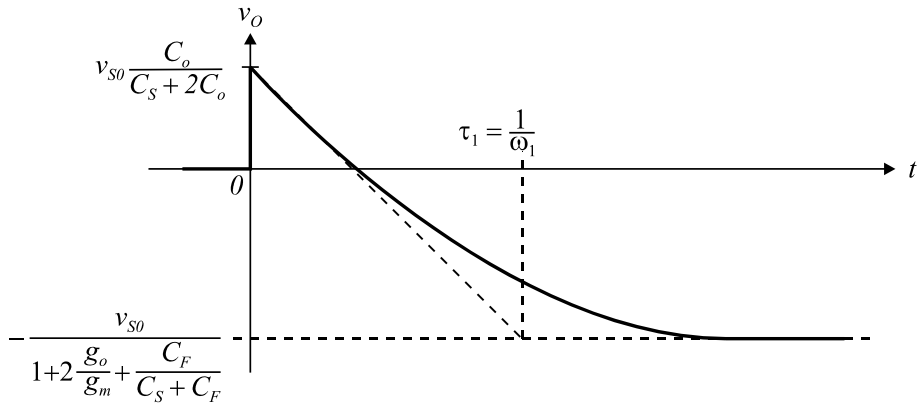

Figure C.3: Settling response given by (C.9)

parasitic output capacitance C_o gives raise to a voltage spike in the opposite direction of the

final voltage. The effect of this is a lengthening of the overall settling time, which can be very problematic in very high speed SI circuits where the storage capacitor C_S might be in the same order of magnitude as the output parasitic capacitor C_o.

Also from Fig. C.3 we notice that the final voltage at the output of CCOP1 or the final input voltage of CCOP2 has been exposed to current transmission errors as described in Chapter B.

Appendix D

Clock Feedthrough and Charge Injection

In this chapter we show how a lumped model for a MOS switch can be derived. The lumped model is the used to derive the switch induced error voltage on a switched capacitor. The switch induced error voltage is investigated for fast and slow switching.

Based on the results for the switched capacitor, the effect of charge injection and clock feedthrough is illustarted for a current copier and an integrator.

D.1 Modeling the MOS switch

Before we can analyze the effect of charge injection and clock Feedthrough we have to have a model of the switch. A switch can be either a NMOS, PMOS or CMOS switch depending on where it is to be used. We will here show how to model a NMOS switch, this model can then be used to model both PMOS and CMOS switches. In Fig. D.1 we have a

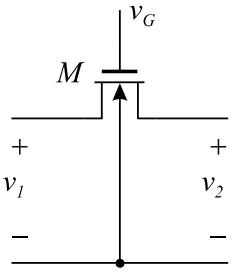

Figure D.1: NMOS transistor used as switch

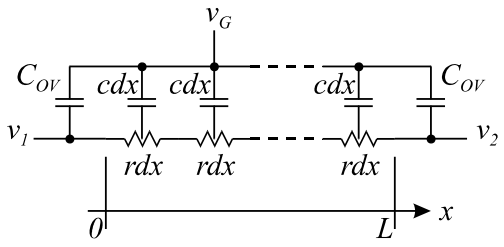

Figure D.2: A distributed RC model for the NMOS transistor

NMOS transistor used as a switch between two points with voltages v_1 and v_2. When the gate-voltage v_G is somewhat higher than v_1 and v_2 (larger than the threshold voltage of the transistor) the switch is on, otherwise the switch is off. At the time when the switch is to be turned off, the two voltages v_1 and v_2 are normally the same. This implies that the transistor $M1$ is operating in its linear region. When $M1$ is in its linear region we can use a distributed model [52][53][54], as shown in Fig. D.2. This figure shows that the transistor consists of two overlap capacitors C_{OV} and of a distributed channel. Here L is the channel length, cdx is the channel capacitance in the infinitesimal channel length dx and rdx is the channel resistance in the infinitesimal channel length dx.

The channel can be broken into infinitesimal sections as shown in Fig. D.3. Based on

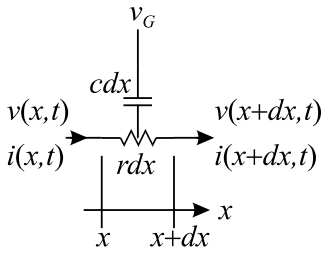

Figure D.3: A small section of the distributed RC model of the NMOS transistor

Fig. D.3 we can now derive a partial differential equation, describing the relationship between the channel voltage $v(x,t)$ and current $i(x,t)$ and the gate voltage v_G. From Fig. D.3 we have that:

$$\begin{aligned} v(x,t) &= v(x+dx,t) + rdx \cdot i(x,t) \\ \Updownarrow & \\ i(x,t) &= -\frac{1}{r} \cdot \frac{\partial v}{\partial x} \end{aligned} \tag{D.1}$$

$$\begin{aligned} i(x+dx,t) &= i(x,t) + cdx \cdot \frac{\partial (v_G - v)}{\partial t} \\ \Updownarrow & \\ \frac{\partial i}{\partial x} &= c \cdot \frac{\partial (v_G - v)}{\partial t} \simeq c \cdot \frac{\partial v_G}{\partial t} \end{aligned} \tag{D.2}$$

the approximation performed in (D.2) is valid because we know that the variation of the channel voltage v is much smaller than the variation of the gate voltage v_G. By combining (D.1) and (D.2) we derive the following equation

$$\frac{\partial^2 v}{\partial x^2} \simeq -rc \cdot \frac{\partial v_G}{\partial t} \tag{D.3}$$

By solving this equation we can get an expression for the channel voltage $v(x,t)$, which when inserted in (D.1) gives the channel current $i(x,t)$. This expression is given by

$$i(x,t) = \left(\frac{x}{L} - \frac{1}{2}\right) C_{OX} \cdot \frac{\partial v_G}{\partial t} \tag{D.4}$$

where C_{OX} is the channel capacitance, i.e. $C_{OX} = C'_{OX} WL$.

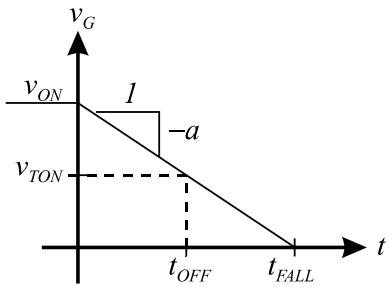

Figure D.4: Voltage at the gate of the switch

In order to simplify the rest of our derivation of the lumped model of the switch, we will assuming that the gate voltage of the switch, when turned off, has the appearance shown in Fig. D.4

When the switch is turned off, the gate voltage v_G goes from a high voltage V_{ON} to zero volts, as shown in Fig. D.4. The slope of the falling gate voltage is shown as $a = -\frac{\partial v_G}{\partial t}$. The time it takes the gate voltage of the switch to reach zero volts is denoted by t_{FALL}. When the gate voltage v_G of the switch falls below the voltage V_{TON} the channel in the switch disappears (the switch is off). The time instant where this happens is denoted by t_{OFF}.

The voltage $V_{T_{ON}}$ is the sum of the input voltage v_{IN} and the voltage dependent threshold voltage, (Bulk effect) $V_T(v_{IN})$, of the switch. Therefore the voltage $V_{T_{ON}}$ can be written as

$$V_{T_{ON}} = v_{IN} + V_T(v_{IN}) \tag{D.5}$$

$$= v_{IN} + V_{T_0} + \gamma\left(\sqrt{2|\Phi| + v_{IN}} - \sqrt{2|\Phi|}\right) \tag{D.6}$$

Because of the bulk effect, the point where the switch turns off will have a nonlinear relationship with the input voltage v_{IN}. This will of course result in some distortion dominated by even order harmonics. Using Taylor expansion, the above equation can be written as

$$V_{T_{ON}} \simeq v_{IN}\left(1 + \frac{\gamma}{2\sqrt{2|\Phi|}}\right) + V_{T_0} \tag{D.7}$$

Assuming that the switch gate voltage has the relationship shown in Fig. D.4, we get from (D.4) that the current at the end points of the switch is given by

$$i(0,t) = +\frac{C_{OX}}{2} \cdot a \tag{D.8}$$

$$i(L,t) = -\frac{C_{OX}}{2} \cdot a \tag{D.9}$$

Based on these equations, the switch can be modelled as shown in Fig. D.5.

The two current sources, each drawing a current $a \cdot C_{OX}/2$, are only active until the switch is turned off. On the other hand the two overlap capacitors, C_{OV}, are active all the time. In Fig. D.5 R is the voltage dependent channel resistance [54] that is given by

$$R = \frac{1}{\beta(v_G - V_{TON})} \tag{D.10}$$

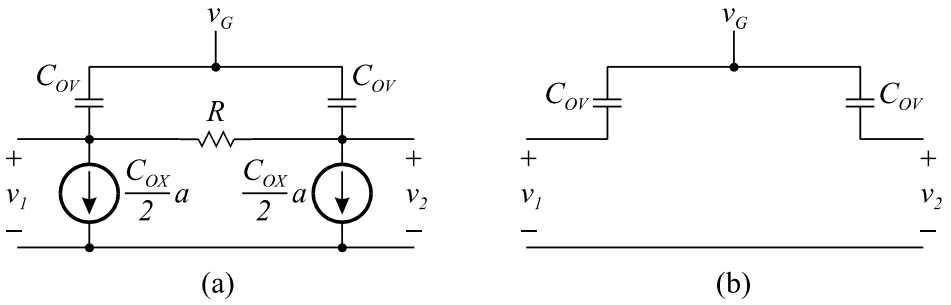

Figure D.5: Lumped Model of a NMOS switch; (a) switch is in its on state; (b) switch is off

D.2 Switched Capacitor

One very simple circuit containing switch induced charge injection and clock feedthrough is shown in Fig. D.6. This circuit shows a signal source, v_{IN}, feeding a capacitor, C_1, through a NMOS switch $M1$. If we exchange the switch with the model that we previously derived, we get the circuit in Fig. D.7. From Fig. D.7 we see that the charge injection and the

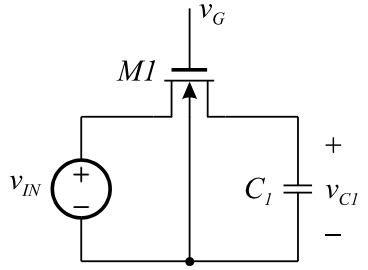

Figure D.6: Voltage signal source, feeding a switched capacitor

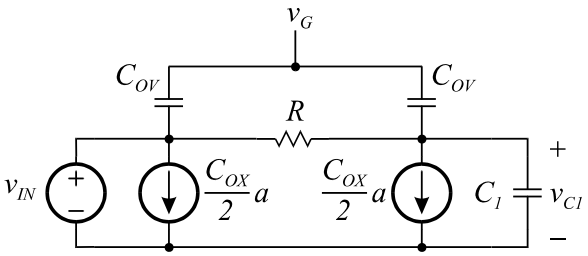

Figure D.7: Switched capacitor with a lumped model for the switch

clock feedthrough is only affected by the part of the switch connected directly to the storage capacitor C_1. Based on this it is now possible to derive the following equation [52][53] , describing the voltage of the storage capacitor after the switch has been turned off, taking into account the voltage dependent channel resistance R.

$$v_C = v_{IN} - \frac{C_{OV} + \frac{C_{OX}}{2}}{C_1}\sqrt{\frac{\pi a C_1}{2\beta}}\,\mathrm{erf}\left((V_{ON} - V_{TON})\sqrt{\frac{\beta}{2aC_1}}\right) - V_{T_{ON}}\frac{C_{OV}}{C_{OV} + C_1} \qquad \text{(D.11)}$$

where $\mathrm{erf}(\cdot)$ is the error function. From the above equation we are now able to investigate the effect of slow and fast turn-off of the switch.

Example D.2.1
This example will illustrate the switch induced error voltage on the capacitor as a function of the turn-off rate a and the input voltage v_{IN}. For this purpose we will make use of the circuit shown in Fig. D.6 and the parameters shown in Table D.1. These parameters are for a standard 2.4μ CMOS process.

Table D.1: Parameters used for the switched capacitor circuit

Parameter	*Value*
V_{ON}	$5.0V$
C_1	$1pF$
W/L	$10\mu m/2.4\mu m$
C_{OV}	$0.0018pF$
C'_{OX}	$0.812fF/\mu m^2$
K'	$57\mu A/V^2$
V_{T_0}	$0.9V$
γ	0.3
$2\lvert\Phi\rvert$	$0.7V$

Slow turn-off When the switch is turned off very slowly i.e. $a \to 0$ we get from (D.11) that the switch induced error voltage is given by

$$v_C - v_{IN} = -V_{TON}\frac{C_{OV}}{C_{OV}+C_1} \tag{D.12}$$

this equation shows that for very slow switching, the switch induced error voltage on the capacitor is dominated by the clock feed-through, through the overlapp capacitor C_{OV}. If we insert (D.7) into the above equation we get that the relationship between the switch induced error voltage and the input voltage v_{IN} is given by

$$v_C - v_{IN} = -v_{IN}\left(1+\frac{\gamma}{2\sqrt{2|\Phi|}}\right)\frac{C_{OV}}{C_{OV}+C_1} - V_{T_0}\frac{C_{OV}}{C_{OV}+C_1} \tag{D.13}$$

Fast turn-off When the switch is turned off very fast i.e. $a \to \infty$ we get from (D.11) that the switch induced error voltage is given by

$$v_C - v_{IN} = -\frac{C_{OV}+\frac{C_{OX}}{2}}{C_1}(V_{ON}-V_{TON}) - V_{TON}\frac{C_{OV}}{C_{OV}+C_1} \tag{D.14}$$

this equation shows that the switch induced error voltage on the capacitor is made from the same contribution as found for slow switching, with the addition of an extra term caused by the charge ejected from the channel of the switch. If we insert (D.7) into the above equation we get that the relationship between the switch induced error voltage and the input voltage v_{IN} is given by

$$v_C - v_{in} = v_{in}\left(1+\frac{\gamma}{2\sqrt{|\Phi|}}\right)\frac{C_{OX}}{2C_1} - (V_{ON}-V_{T_0})\frac{C_{OX}}{2C_1} \tag{D.15}$$

In Fig. D.8 the switch induced error voltage is illustrated, for different switching ratios, as a function of the input voltage. These curves have been found by performing a circuit

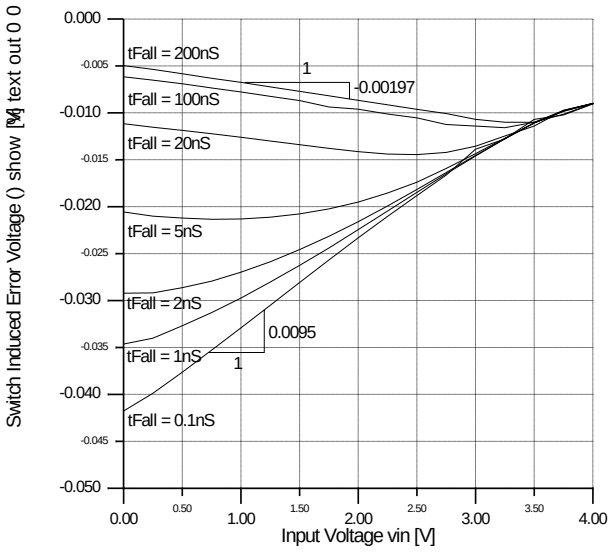

Figure D.8: Switch induced error voltage for different switching ratios

simulation of the circuitry shown in Fig. D.6 using PSPICE. We notice that for input voltages larger than approximately $3.5V$, all of the curves join with the same switch induced error voltage. For an input voltage of $3.5V$ we have that the voltage V_{TON} is equal to $V_{TON} = 4.76V$ i.e. close to the voltage V_{ON}. Therefore the largest input voltage the switch can handle is $3.5V$.

If we insert the values shown in Table D.1 into the equations (D.14) and (D.15) we can predict that the switch induced error voltage for slow switching is given by

$$v_C - v_{IN} = -v_{IN} \cdot 0.00212 - 0.00162V \tag{D.16}$$

and for fast switching

$$v_C - v_{IN} = v_{IN} \cdot 0.01149 - 0.04V \tag{D.17}$$

By comparing these predictions with the actual simulations shown in Fig. D.8 we see that they are fairly accurate.

In general terms we have seen that the switch induced error Δ can be written as

$$\Delta = \alpha \cdot v_{IN} - \beta \tag{D.18}$$

■

D.3 Current Copier

Until now we have discussed how to model the switch and how this model can be used to determine the switch induced error voltage on switched-capacitor. Based on these previous results we are now able to determine how the switch affects the behavior of a single current copier. In Fig. D.9 we have a current copier where the feedback switch is shown as a MOS transistor M_S and the other switches are shown as ideal switches. This is because it is only the feed-back switch that causes switch induced errors on the storage capacitor C_1. The reason for this is that this switch is turned off before any of the other switches.

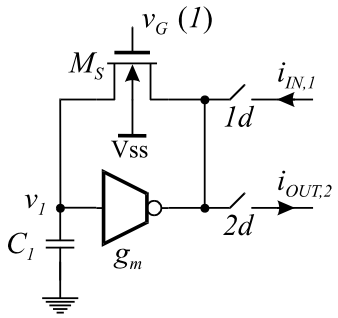

Figure D.9: A current copier showing the switch that causes errors

Assuming that we turn-off the feedback-switch very fast, we have seen from the previous sections that there will be little or no equalization through the switch on-resistance. Therefore half of the charge from the switch is dumped on the storage capacitor C_1 leading to an error voltage equal to (D.15).

This error voltage will give raise to both linear and non-linear effects at the output of the current copier.

If we however turn-off the switch rather slowly there will be almost no error voltage on the storage capacitor C_1 because the transconductor will equalize the error [55].

D.3.1 Linear effects

Assuming that the transconductor is perfectly linear and has a transconductance of g_m, the signal voltage on the storage capacitor at the end of the copy-phase is given by

$$v_{1,1} = \frac{i_{IN,1}}{g_m} \tag{D.19}$$

when the feedback switch has been turned off, we have a switched induced error voltage at the storage capacitor given by (D.18), which implies that the voltage at the storage capacitor has changed to

$$v_{1,1} = \frac{i_{IN,1}}{g_m}(1+\alpha) - \beta \tag{D.20}$$

Therefore the output current in the hold-phase is given by

$$\underline{i_{OUT,2} = -i_{IN,1}(1+\alpha) + g_m\beta} \tag{D.21}$$

which shows that the output current will be a scaled version of the input signal and some offset. The actual scaling factor will depend upon the slope of the clock signal used for driving the switch. For very fast switching we have seen that $\alpha > 0$, which implies that the scaling factor will be larger than one !. And for slow switching we have that $\alpha < 0$, which implies that the scaling factor will be smaller than one !.

D.4 Integrator

In this section will try to describe how clock feedthrough and charge injection affect the operation of a SI integrator. The analysis is based on the results found in the previous section. In Fig. D.10 we have shown a SFG representing a SI integrator including the effects of clock feedthrough and charge injection. Using Mason formula and the SFG in Fig. D.10,

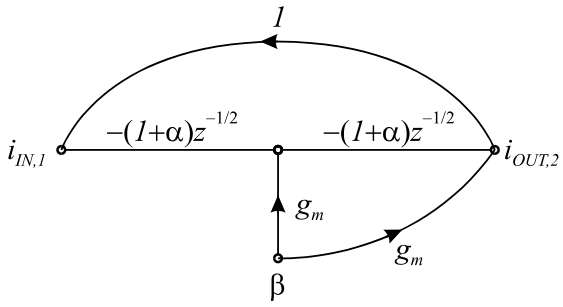

Figure D.10: SFG showing the effect of clock feedthrough and charge injection in SI integrators.

which represents the series connection of two current copiers, we get that the transfer function from the input current $i_{IN,1}$ and the offset β to the output current $i_{OUT,1}$ is given by

$$i_{OUT,2} = i_{IN,1} \underbrace{\frac{(1+\alpha)^2 z^{-1}}{1-(1+\alpha)^2 z^{-1}}}_{H_i(z)} + \beta g_m \underbrace{\frac{1-(1+\alpha) z^{-1/2}}{1-(1+\alpha)^2 z^{-1}}}_{H_\beta(z)} \tag{D.22}$$

Because β is an offset term, independent of the frequency we have that its contribution to the output signal of the integrator can be found by setting $z = 1$ (DC) in the transfer function $H_\beta(z)$.

$$\beta g_m H_\beta(z)|_{z=1} = \frac{\beta g_m}{2+\alpha} \simeq \frac{\beta g_m}{2} \tag{D.23}$$

which shows that it contributes with a small offset at the output of the integrator.

We also notice that clock feedthrough and charge injection affects the signal transfer function $H_i(z)$. The poles of the transferfunction $H_i(z)$ are located at

$$z_{pole} = (1+\alpha)^2 \tag{D.24}$$

from this equation we see that for fast switching i.e. $\alpha > 0$ the pole of the integrator is expected to lie outside the unity circle making the integrator unstable.

A simulation of the impulse response of a SI integrator using fast switching shows that the output of the integrator is not constant with time, but slowly ramps towards infinity and eventually saturates at the bias current. This behavior clearly verifies that the integrator is unstable and that the pole of the integrator is located outside the unit circle.

Appendix E

Noise in Sampled Data Systems

The subject of this appendix is to give the necessary background for calculating the noise in analog sampled data systems [56]. This applies to both switched capacitor [57] and switched current circuits [13]. This chapter is specially aimed at the treatment of optimization of SI circuits given in Chapter 5.

E.1 Introduction

To describe a stationary statistical signal we make use of the autocorrelation function $R(\tau) = E\{x(t)x(t+\tau)\}$ and the power spectral density $S(f)$ which is the fourier transformed of the autocorrelation function [58].

The power of a noise signal is found by integrating the noise power spectral density over the frequency band of interest. The noise must be bandlimited, otherwise we get infinite power which is physically unrealizable.

White noise is the term applied to any zero-mean random process whose power spectral density is a constant (a mathematical ideallity).

Example E.1.1
In order to illustrate the above terms we will make use of a familiar example. We will find the mean square voltage across a noiseless capacitor shunted by a noisy resistor. The circuit we are describing is shown in Fig. E.1. The thermal double sided power spectral density of

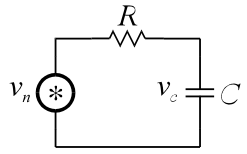

Figure E.1: Capacitor shunted by a noisy resistor

a noisy resistor is normally written as [59]

$$S_{vn}(f) = 2kTR \tag{E.1}$$

which corresponds to an autocorrelation function given by [58]

$$R_{vn}(\tau) = 2kTR \cdot \delta(\tau) \tag{E.2}$$

This equation shows that *there is no correlation between two noise samples taken from a white noise source at two distinct times*. The power spectral density of the noise voltage across the capacitor can be found by the following equation [58]

$$S_{vc}(f) = S_{vn}(f) \cdot |H(f)|^2 \tag{E.3}$$

where $H(f)$ is the transfer function from the resistor noise source to the voltage across the capacitor. We have that

$$|H(f)|^2 = \frac{1}{1 + \left(\frac{f}{f_o}\right)^2} \tag{E.4}$$

Also the autocorrelation of the noise voltage across the capacitor is given by [58]

$$R_{vc}(\tau) = R_{vn}(\tau) \otimes R_h(\tau) \tag{E.5}$$

here $\otimes$ is the convolution operator and $R_h(\tau)$ is the autocorrelation of the impulse response corresponding to the transfer function $H(f)$. The autocorrelation function $R_h(\tau)$ can be found as

$$R_h(\tau) = \frac{1}{2RC} \cdot e^{-\frac{|\tau|}{RC}} \tag{E.6}$$

By combining (E.2) and (E.6) as shown in (E.5) we get that

$$R_{vc}(\tau) = \frac{kT}{C} \cdot e^{-\frac{|\tau|}{RC}} \tag{E.7}$$

The mean squared of the noise voltage across the capacitor can be found as $R_{vc}(0)$ which is

$$R_{vc}(0) = E\{vc^2\} = \frac{kT}{C} \tag{E.8}$$

This result could also have been found by integrating the power spectral density of the noise voltage across the capacitor $S_{vc}(f)$ over all frequencies. This is shown in the following equations

$$\begin{aligned} E\{vc^2\} &= \int_{-\infty}^{+\infty} S_{vn}(f) \cdot |H(f)|^2 df && \text{(E.9)} \\ &= 2kTR \int_{-\infty}^{+\infty} \frac{df}{1 + \left(\frac{f}{f_o}\right)^2} && \text{(E.10)} \\ &= 2kTR \cdot \frac{1}{2RC} && \text{(E.11)} \\ &= \frac{kT}{C} && \text{(E.12)} \end{aligned}$$

The above calculations show that the mean square of the noise voltage across the capacitor is independent of the resistor. In general terms *this is not correct* which can easily be seen from the fact that a zero resistance $R = 0$ intuitively should give a zero voltage across the capacitor also a infinitely small capacitor should not give an infinite mean squared voltage across the capacitor this is physically not possible.

The reason that the limiting cases $R \to 0$ and $C \to 0$ do not hold is caused by the assumption that the power spectral density of the thermal noise generated in the resistor was not bandlimited i.e. it was assumed to be a white noise.

The term white noise is a mathematical ideallity that is physically not realizable, one should be aware of that.

A general expression for the mean squared voltage across the capacitor can be found by correcting the power spectral density of the thermal noise from the resistor (E.1) for quantum effects. It can be shown that the power spectral density should be multiplied by the correction factor [59][60]

$$\frac{\frac{hf}{kT}}{e^{\frac{hf}{kT}}-1} \tag{E.13}$$

where h is planck's constant and f is the frequency. The 3dB cut-off frequency of this correction factor is found at approximately 4000GHz, which is indeed a high frequency. Therefore in practical situations the white noise source is not bandlimited by quantum effects but by the circuit itself, and the correction factor can be omitted. Using the above correction it can be shown that the mean squared of the noise voltage across an isolated resistor ($C \to 0$) is given by

$$E\{v^2\} = R \cdot \frac{2}{3} \cdot \frac{(\pi kT)^2}{h} \tag{E.14}$$

Assuming that it could be possible to isolate a resistor of $1M\Omega$ at a temperature of 27^oC, the RMS noise voltage across the resistor would be $0.17V$ ■

The above examples have introduced the terms necessary for describing noise, we have also shown that the concept of noise bandwidth which is very important when dealing with noise.

E.2 Sampling of Noise

In electronic circuits the noise sources are bandlimited by the signal processing system itself. Also the limiting cases $R \to 0$ and $C \to 0$ do not occur, therefore it is not necessary to take into account quantum effects when calculating the noise powers.

The bandlimitation in the signal processing circuits is determined by the requirements for the settling behavior, this is true both for switched capacitor and switched current circuits. Because of this the bandlimitation of the signal processing circuit itself is most often somewhat higher that the sampling frequency f_s of the system.

The effect of sampling a bandlimited analog noise source can be described by sampling the autocorrelation function [58]. This is shown in the following equation.

$$r_{nb}(t) = R_{nb}(t) \cdot \delta_T(t) \text{ , where } \delta_T(t) = \sum_{n=-\infty}^{+\infty} \delta(t-nT) \tag{E.15}$$

Here $R_{nb}(t)$ is the autocorrelation of the bandlimited analog noise source and $r_{nb}(t)$ is the autocorrelation for the sampled analog noise (digital noise). The sampling is performed by an infinite series of delta functions $\delta_T(t)$ located at the different sampling instances.

The power spectrum $s_{nb}(f)$ of the sampled analog noise source can now be found by fourier transforming the autocorrelation function $r_{nb}(t)$ of the sampled analog noise.

$$\begin{aligned} s_{nb}(f) &= S_{nb}(f) \otimes f_s \delta_{f_s}(f) \text{ , where } f_s = \frac{1}{\Delta T} \\ &= f_s \sum_{n=-\infty}^{+\infty} S_{nb}(f - nf_s) \end{aligned} \tag{E.16}$$

We have assumed that the analog noise was bandlimited, it can therefore be written as

$$S_{nb}(f) = S_n(f) \cdot |B(f)|^2 \tag{E.17}$$

where $S_n(f)$ is the power spectral density of the analog noise source before it is bandlimited by the signal processing system $|B(f)|^2$. If we insert (E.17) into (E.16) we get that the power spectrum of the sampled analog noise is given by

$$\underline{s_{nb}(f) = f_s \sum_{n=-\infty}^{+\infty} S_n(f - nf_s)|B(f - nf_s)|^2} \tag{E.18}$$

This equation shows that if the bandwidth of the analog noise is greater than half the sampling frequency, there will be some aliasing of noise into the frequency band $[-f_s/2; +f_s/2]$.

E.3 Sampling of White Noise

An analog white noise source has a power spectral density that is independent of the frequency i.e. it can be written as

$$S_n^w(f) = S_n^w \tag{E.19}$$

if we insert (E.19) into (E.18) we get that the power spectrum of a sampled bandlimited analog white noise is given by

$$\underline{s_{nb}(f) = S_n^w f_s \sum_{n=-\infty}^{+\infty} |B(f - nf_s)|^2} \tag{E.20}$$

Assuming that the bandlimiting function $B(f)$ is a brick wall filter, the concept of undersampling white noise is shown in Fig. E.2. The sampling of the bandlimited noise has the effect

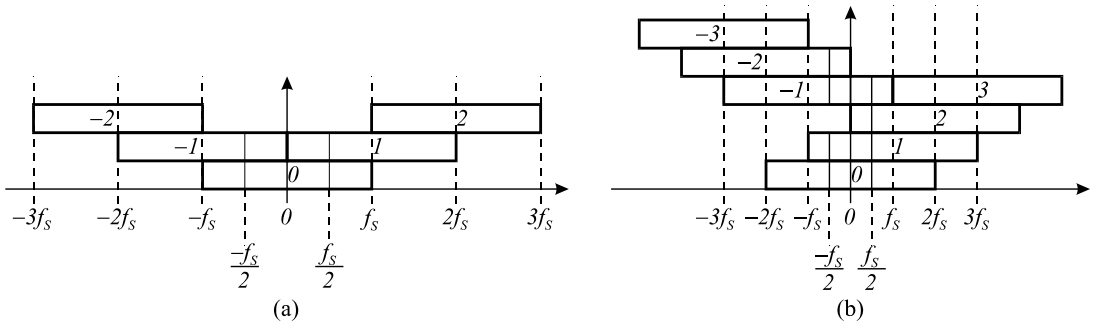

Figure E.2: Illustration of the undersampling of bandlimited white noise: (a) bandwith equal to sampling frequency; (b) bandwidth equal to twice sampling frequency

of generating replicas, $(-3, -2, -1, 1, 2, 3)$ around multiples of the sampling frequency, of the bandlimited noise (replica 0). When the noise is under sampled these replicas will overlap as shown in Fig. E.2 and the total noise power found in the frequency range $[-f_S/2; +f_S/2]$ (shown as the gray areas) will be equal to the total noise power of the bandlimited noise itself i.e. the effect of undersampling bandlimited white noise is that all of the noise power is folded down into the frequency band $[-f_S/2; +f_S/2]$.

Based on the fact that all of the noise power is folded down into the frequency band $[-f_S/2; +f_S/2]$ and on the fact that the resulting power spectrum of the undersampled bandlimited white noise will be approximately white we can now conclude that the power spectrum of the sampled white noise must be given by

$$s_{nb}(f) = S_n^w \cdot \text{BWN} \text{ , where BWN} = \int_{-\infty}^{+\infty} |B(f)|^2 df \tag{E.21}$$

In the above equation BWN represents the double sided equivalent noise bandwidth.

Now we have an easy way of calculating the power spectrum of a sampled analog noise source, all we have to do is to calculate the double sided noise bandwidth BWN. In Table E.1 we have calculated this noise bandwidth BWN for lowpass filters of different orders i.e. with multiple poles at the cut-off frequency using the following equation.

$$\text{BWN} = \int_{-\infty}^{+\infty} \frac{df}{\left(1 + \left(\frac{f}{f_o}\right)^2\right)^n} \tag{E.22}$$

Table E.1: Noise Bandwidth BWN, for lowpass filters of order n.

Order n	Noise bandwidth BWN
1	$\frac{\omega_0}{2}$
2	$\frac{1}{2}\frac{\omega_0}{2}$
3	$\frac{3}{8}\frac{\omega_0}{2}$
4	$\frac{5}{16}\frac{\omega_0}{2}$

Example E.3.1
This example will illustrate the effect of undersampling a white noise source that has been bandlimited by a first order lowpass filter with the transferfunction shown below

$$|B(f)|^2 = \frac{1}{1 + \left(\frac{f}{f_0}\right)^2} \tag{E.23}$$

From (E.20) we see that the shape of the power spectrum of the sampled noise is determined by the sum

$$\sum_{n=-\infty}^{+\infty} |B(f - nf_s)|^2 \tag{E.24}$$

In Fig. E.3 I have plotted the above sum for two different ratios between of cut-off frequency and sampling frequency.

The shape of the sum shown in Fig. E.3 tells us that the power spectrum of the sampled noise will be approximately white. This especially true if we increase the degree of undersampling.

From Fig. E.3 we see that if the bandwidth and the sampling frequency are equal the sum is approximately equal to π. We also see that when the bandwidth is twice the sampling frequency the sum is approximately equal to 2π. For a first order lowpass filter we therefore conclude that

$$\sum_{n=-\infty}^{+\infty} |B(f - nf_s)|^2 \simeq \pi \frac{f_0}{f_S} \tag{E.25}$$

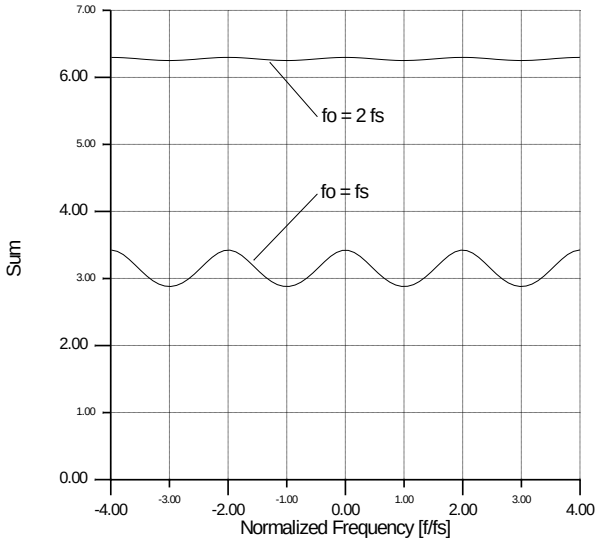

Figure E.3: Sum of the replica of the squared magnitude of the transfer function for a 1st order lowpass filter

If we insert this relationship into (E.20) we get that the power spectrum is given by

$$s_{nb}(f) = S_n^w f_S \pi \frac{f_0}{f_S} = S_n^w \pi f_0 = S_n^w \frac{\omega_0}{2} \tag{E.26}$$

This is exactly the same result as we would have got if we had used (E.21) on a first order lowpass filter i.e. the first row in Table E.1 ■

E.4 Sampling of 1/f Noise

Low frequency $1/f$ noise has a power spectral density that can be written as

$$S_n^{1/f}(f) = \frac{K}{|f|} \tag{E.27}$$

if we insert this equation into (E.18) we get that the power spectrum of the sampled $1/f$ noise is given by

$$\underline{s_{nb}^{1/f}(f) = f_s \sum_{n=-\infty}^{+\infty} \frac{K}{|f - nf_s|} |B(f - nf_s)|^2} \tag{E.28}$$

In the above equation the transfer function $B(f)$ is the bandlimitation that the $1/f$ noise is exposed to before it is sampled. The cut-off frequency of this bandlimitation will in most sampled data systems be somewhat higher than the sampling frequency. Therefore the effect of this bandlimitation on the sampled $1/f$ noise will be very small at low frequencies and we will assume that it can be neglected.

Based on this assumption we have that the power spectrum of the sampled $1/f$ noise is given by

$$s_{nb}^{1/f}(f) = S_n^{1/f} \cdot f_S, f \in [-f_s/2; +f_s/2] \tag{E.29}$$

The noise power of the sampled $1/f$ in the frequency band $[f_1; f_2]$ is given by

$$P_n = \frac{2}{f_S}\int_{f_1}^{f_2} s_{nb}^{1/f}(f)df = \frac{2}{f_S}\int_{f_1}^{f_2} S_n^{1/f} f_S df = 2\int_{f_1}^{f_2} S_n^{1/f} df \tag{E.30}$$

Example E.4.1
This example will illustrate the effect of sampling a $1/f$ noise source that has been bandlimited by a first order lowpass filter with the transferfunction shown below

$$|B(f)|^2 = \frac{1}{1+\left(\frac{f}{f_0}\right)^2} \tag{E.31}$$

In Fig. E.4 I have plotted (E.28) with $K = 1$ for this first order bandlimitation.

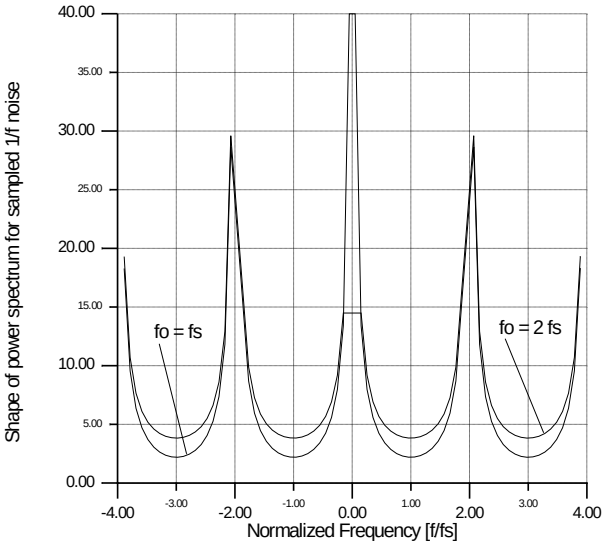

Figure E.4: Shape of the power spectrum for a sampled $1/f$ noise source

From Fig. E.4 we see that the aliasing of the sampled $1/f$ noise causes the noise floor to raise. A wide bandwidth of the bandlimitation gives a higher noise floor. The level of this noise floor is however small compared to the amplitude of the $1/f$ spectrum at low frequencies, we will therefore assume that this raise in the noise floor can be ignored. ■

E.5 Noise power at the output of a large system

In most sampled data systems there will be more than one noise source contributing to the overall noise at the output of the system. Considering only sampled noise sources it is fairly easy to calculate the noise power at the output of any sampled data system. Assuming that all the noise sources are uncorrelated, the noise power at the output of the system can be found by integrating the sum of products of the power spectrum of the sampled noise sources and their respective numerically squared transfer functions to the output.

For white noise sources the noise power at the output of the system is described by the following equation

$$P_n = \frac{1}{f_s}\int_{-f_s/2}^{+f_s/2} \left(s_{n1}^w(f)|H_{n1}(f)|^2 + \cdots + s_{nm}^w(f)|H_{nm}(f)|^2\right) df \tag{E.32}$$

in this equation $H_{ni}(f)$ is the transfer function from the white noise source s_{ni}^w to the output. Using Parsevals theorem the above equation can be rewritten as

$$P_n = s_{n1}^w \sum_{k=0}^{+\infty} h_{n1}^2[k] + \cdots + s_{nm}^w \sum_{k=0}^{+\infty} h_{nm}^2[k] \tag{E.33}$$

in this equation $h_{ni}[k]$ represents the impulse response sequence from the white noise source s_{ni}^w to the output.

For lowfrequency $1/f$ noise sources the noise power at the output of the system in the frequency band $[f_1; f_2]$ is given by

$$P_n = \frac{2}{f_s} \int_{f_1}^{f_2} \left(s_{n1}^{1/f}(f)|H_{n1}(f)|^2 + \cdots + s_{nm}^{1/f}(f)|H_{nm}(f)|^2 \right) df \tag{E.34}$$

E.6 Correlated Double Sampling (CDS) of $1/f$ Noise

In switched current circuits we often have that the lowfrequency $1/f$ noise is exposed to correlated double sampling (CDS). Correlated double sampling has its origin in the current copier cell, and has the effect of frequency shaping the $1/f$ noise with the following transferfunction

$$H(z) = 1 - z^{-1/2} \tag{E.35}$$

Correlated double sampling is also often used in switched-capacitor circuits for suppressing offset voltages and low frequency $1/f$ noise. If we insert $z = e^{j2\pi f \Delta T}$ into (E.35) we get that

$$|H(f)|^2 = 4 \cdot sin^2(\frac{\pi}{2} \cdot \frac{f}{f_s}) \tag{E.36}$$

Based on (E.27) and (E.29) we have that the power spectrum of a sampled $1/f$ noise source can be written as

$$s_n^{1/f}(f) = f_s \cdot \frac{K}{|f|} \tag{E.37}$$

Using (E.34) we can now calculated the noise power of the sampled $1/f$ noise with CDS, we get

$$\begin{aligned}
\underline{P_n^{1/f}} &= \frac{2}{f_s} \int_0^{f_s/2} s_n^{1/f}(f)|H(f)|^2 df && \text{(E.38)} \\
&= 4K f_s \cdot \frac{2}{f_s} \int_0^{f_s/2} \frac{sin^2(\frac{\pi}{2} \cdot \frac{f}{f_s})}{f} df && \text{(E.39)} \\
&= 8K \int_0^{\pi/4} \frac{sin^2(u)}{u} du && \text{(E.40)} \\
&= 8K \cdot 0.2784 && \text{(E.41)} \\
&= \underline{2.2272K} && \text{(E.42)}
\end{aligned}$$

Appendix F

Matching Errors

It is of great interest to know how matching errors influence on the behavior of switched current circuits. This is so because matching will determine how accurately we fx. can make possible filter coefficients e.t.c. Matching errors can also be a source of distortion.

In this appendix we will illustrate how mismatch between different transistor parameters influences the performance of a current copier. We will also show how biasing and transistor geometry affects the statistical properties of the matching mechanisms.

F.1 Introduction

To illustrate the effect of matching errors we will make use of the current copier shown in Fig. F.1 On clock phase 1 (Copy phase) the switch S_1 and S_2 are closed. The effect of this

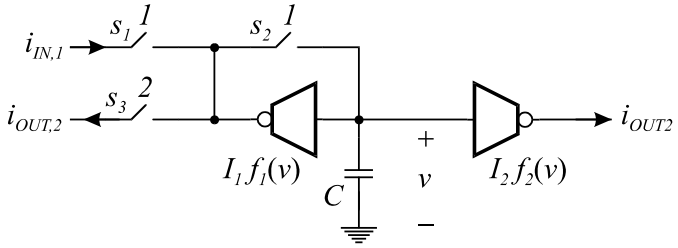

Figure F.1: A Current Copier with an extra current output

is that the current copier acts as a current mirror between $i_{IN,1}$ and i_{OUT2}.

From Fig. F.1 we get the following relationship for the output current.

$$i_{OUT2} = -I_2 f_2 \left(f_1^{-1}(\frac{i_{IN,1}}{I_1}) \right) \tag{F.1}$$

this equation shows that if the two nonlinearities $f_1(\cdot)$ and $f_2(\cdot)$ are the same we would get a perfectly linear relationship between the output current and the input current, and this relationship would be given by

$$i_{OUT2} = -i_{IN,1} \frac{I_2}{I_1} \tag{F.2}$$

Because of mismatch errors the two nonlinearities $f_1(\cdot)$ and $f_2(\cdot)$ are not the same and we do not necessarily get a linear relationship between the input current $i_{IN,1}$ and the output current i_{OUT2}. Such a situation is best illustrated by a small example.

Example F.1.1
We will now assume that the transconductors in Fig. F.1 are implemented using simple MOS transistors. This leads to the circuit shown in Fig. F.2. From Fig. F.2 we get the following

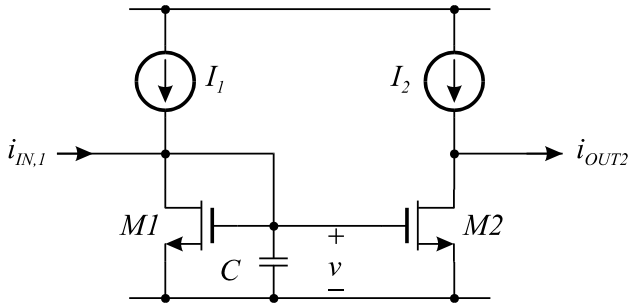

Figure F.2: A simple implementation of a Current Copier; with a extra current output; in its copy phase i.e. phase 1

relationships for the voltage and currents in the current copier

$$\begin{aligned} v &= V_{T_1} + \sqrt{\frac{2(I_1 + i_{IN,1})}{\beta_1}} \\ i_{OUT2} &= I_2 - \frac{\beta_2}{2}(v - V_{T_2})^2 \end{aligned} \tag{F.3}$$

From (F.3) we get that the output current can be written as

$$i_{OUT2} = I_2 - \frac{\beta_2}{2}\left(\sqrt{\frac{2(I_1 + i_{IN,1})}{\beta_1}} + \underbrace{(V_{T_1} - V_{T_2})}_{\Delta V_T}\right)^2 \tag{F.4}$$

$$= \underbrace{\beta_2\left(\frac{I_2}{\beta_2} - \frac{I_1}{\beta_1}\right)}_{\text{1st Term}} - \underbrace{I_{IN,1}\frac{\beta_2}{\beta_1}}_{\text{2nd Term}} - \underbrace{\frac{\beta_2}{2}\Delta V_T^2}_{\text{3rd Term}} - \underbrace{\beta_2 \Delta V_T \sqrt{\frac{2(I_1 + i_{IN,1})}{\beta_1}}}_{\text{4th Term}} \tag{F.5}$$

From this equation we make the following conclusions

- **Scaling** errors are caused by mismatch in the transconductance parameter β as seen from the 2nd term.
- **Offset** errors are caused by mismatch in the transconductance parameter β and in the threshold voltage ΔV_T as seen from the 1st and the 3rd term.
- **Distortion** is caused by the mismatch in threshold voltage ΔV_T as seen from the 4th term. The amplitude of the harmonics can be found by Taylor expanding the 4th term.

A somewhat similar calculation has been performed by others [51][6][7] ■

Scaling errors and offset errors are in most situations less critical than distortion errors. Therefore in order to reduce the distortion in switched current circuits we have to match the components as well as possible and at the same time we note that distortion only arises because of mismatch when the transconductors are nonlinear. Therefore it is advisable to use linearized transconductors for low distortion switched current circuits.

The factors determining the actual mismatch can be divided into systematic errors and statistical errors [61].

The systematic errors are such as etching errors and lithographic errors e.t.c. These errors can be reduced by using unity transistors [61].

The statistical errors are among other things caused by statistical variations of the oxide thickens, the dopant atoms in the bulk and of the mobility [62][63].

F.2 Single MOS transistor

In the previous analysis we have assumed that the MOS transistors are operating in strong-inversion and saturation and that the relationship between drain current and gate-source voltage is given by

$$i_D = \frac{\beta}{2}\left(v_{GS} - V_T\right)^2 \tag{F.6}$$

in this equation we will assume that β and V_T are stocastic variables

The variance of the drain current i_D for a given gate–source voltage v_{GS} can be calculated by Taylor expanding (F.6) around the mean value of β and V_T. The mean value of β and V_T is denoted by $\overline{\beta}$ and $\overline{V_T}$. Using this approach we get the following relationship

$$i_D = \overline{i_D} + \left(\beta - \overline{\beta}\right)\left.\frac{\partial i_D}{\partial \beta}\right|_{\overline{\beta},\overline{V_T}} + \left(V_T - \overline{V_T}\right)\left.\frac{\partial i_D}{\partial V_T}\right|_{\overline{\beta},\overline{V_T}} \tag{F.7}$$

from this equation the variance of the drain current can be found as

$$\sigma^2_{i_D} = \sigma^2_\beta\left(\left.\frac{\partial i_D}{\partial \beta}\right|_{\overline{\beta},\overline{V_T}}\right)^2 + \sigma^2_{V_T}\left(\left.\frac{\partial i_D}{\partial V_T}\right|_{\overline{\beta},\overline{V_T}}\right)^2 + \left(\left.\frac{\partial i_D}{\partial \beta}\right|_{\overline{\beta},\overline{V_T}}\right)\left(\left.\frac{\partial i_D}{\partial V_T}\right|_{\overline{\beta},\overline{V_T}}\right) Cov(\beta, V_T) \tag{F.8}$$

Both theoretical and experimental results have shown that the correlation between β and V_T is very small [62] and can be considered as zero. Therefore we have that $Cov(\beta, V_T) \simeq 0$. From (F.6) we get that

$$\overline{i_D} = \frac{\overline{\beta}}{2}\left(v_{GS} - \overline{V_T}\right)^2 \tag{F.9}$$

$$\left.\frac{\partial i_D}{\partial \beta}\right|_{\overline{\beta},\overline{V_T}} = \frac{1}{2}\left(v_{GS} - \overline{V_T}\right)^2 \tag{F.10}$$

$$\left.\frac{\partial i_D}{\partial V_T}\right|_{\overline{\beta},\overline{V_T}} = -\overline{\beta}\left(v_{GS} - \overline{V_T}\right) \tag{F.11}$$

if we insert these equations into (F.8) we get that variance of the drain current can be written as

$$\sigma^2_{i_D} = \sigma^2_\beta\frac{1}{4}\left(v_{GS} - \overline{V_T}\right)^4 + \sigma^2_{V_T}\overline{\beta}^2\left(v_{GS} - \overline{V_T}\right)^2 \tag{F.12}$$

therefore the relative variance of the drain current can be written as

$$\underline{\frac{\sigma^2_{i_D}}{\overline{i_D}^2} = \frac{\sigma^2_\beta}{\overline{\beta}^2} + \frac{\sigma^2_{V_T}}{\overline{V_T}^2}\frac{4}{\left(\frac{v_{GS}}{\overline{V_T}} - 1\right)^2}} \tag{F.13}$$

this equation shows that it is very important that the gate-source voltage is made somewhat larger than the threshold voltage in order to reduce the relative error of the threshold voltage.

Put in an other way; MOS transistors with very low saturation voltages $(v_{GS} - V_T)$ have very poor matching characteristics due to variations in the threshold voltage.

The transconductance parameter β is determined by

$$\beta = \frac{W}{L}\mu C'ox \tag{F.14}$$

from this equation we get that the relative variance of β is given by (assuming that all of the parameters are uncorrelated)

$$\frac{\sigma_\beta^2}{\overline{\beta}^2} = \underbrace{\frac{\sigma_W^2}{\overline{W}^2} + \frac{\sigma_L^2}{\overline{L}^2}}_{\text{1st Term}} + \underbrace{\frac{\sigma_\mu^2}{\overline{\mu}^2} + \frac{\sigma_{C'ox}^2}{\overline{C'ox}^2}}_{\text{2nd Term}} \tag{F.15}$$

the 1st term in the above equation represents the statistical edge variations and the 2nd term represents the statistical variations in the mobility and in the gate oxide. It can be shown [62] that the relative variance of the transconductance parameter β and of the threshold voltage V_T can be represented as

$$\frac{\sigma_\beta^2}{\overline{\beta}^2} = \frac{\sigma_W^2}{\overline{W}^2} + \frac{\sigma_L^2}{\overline{L}^2} + \frac{A_\beta^2}{\overline{W}\,\overline{L}} \tag{F.16}$$

$$\frac{\sigma_{V_T}^2}{\overline{V_T}^2} = \frac{A_{V_T}^2}{\overline{W}\,\overline{L}} \tag{F.17}$$

Example F.2.1
For a typical $3\mu m$ CMOS process [62] we have that:

$\sigma_L \simeq \sigma_W \simeq 0.01\mu m$ to $0.03\mu m$
$A_\beta = 0.006\mu m$
$A_{V_T}^{NMOS} = 0.016V\mu m$
$A_{V_T}^{PMOS} = 0.031V\mu m$

The PMOS transistor in this process has an additional threshold adjust implant, which causes a larger threshold voltage mismatch for the PMOS transistor than for the NMOS transistor.

For A PMOS transistor with the following parameters:
$W = 33\mu m$, $L = 3\mu m$, $\overline{V_T} = 0.5V$ and $v_{GS} - V_T = 0.1V$
we get the following matching properties:

$$\frac{\sigma_\beta^2}{\overline{\beta}^2} = \left(\frac{0.02\mu m}{33\mu m}\right)^2 + \left(\frac{0.02\mu m}{3\mu m}\right)^2 + \left(\frac{0.006\mu m}{3\mu m \cdot 33\mu m}\right)^2 = 44.81543 \cdot 10^{-6}$$

$$\frac{\sigma_{V_T}^2}{\overline{V_T}^2} = \frac{(0.031V\mu m)^2}{3\mu m \cdot 33\mu m} = 9.70707 \cdot 10^{-6}V^2$$

If we insert the above results into (F.13) we get that the relative variance of the drain current is given by

$$\frac{\sigma_{i_D}^2}{\overline{i_D}^2} = 44.81543 \cdot 10^{-6} + 9.70707 \cdot 10^{-6}V^2\frac{4}{(0.2V)^2} = 44.81543 \cdot 10^{-6} + 970.7070 \cdot 10^{-6}$$

this shows that it is the threshold voltage that is the dominating error source because of the low saturation voltage. The relative standarddeviation of the drain current is now given by

$$\frac{\sigma_{i_D}}{\overline{i_D}} = 0.03187 \sim 3.2\%$$

■

F.3 Parallel connection of unity transistors

One way of reducing both systematic and statistical matching errors is by using unity transistors [61]. In Fig. F.3 we have connected N unity transistors in parallel giving a equivalent of one transistors N times wider than a unity transistor.

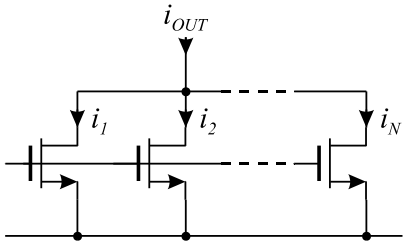

Figure F.3: Parallel connection of N unity transistors

From Fig. F.3 we see that the output current is given by

$$i_{OUT} = i_1 + i_2 + \cdots + i_N \tag{F.18}$$

and that the mean value of the output current is given by

$$\overline{i_{OUT}} = N\overline{i_o} \tag{F.19}$$

where $\overline{i_o}$ is the nominal output current in each transistor. Assuming that the transistors are uncorrelated, the variance of the output current is given by

$$\sigma^2_{i_{OUT}} = N\sigma^2_{i_0} \tag{F.20}$$

by combining (F.19) and (F.20) we get that the relative standarddeviation of the output current, from the parallel connected unity transistors, is given by

$$\frac{\sigma_{i_{OUT}}}{\overline{i_{OUT}}} = \frac{1}{\sqrt{N}}\frac{\sigma_{i_o}}{\overline{i_o}} \tag{F.21}$$

This equation shows that the relative standarddeviation of the output current is reduced by the square root of the number of unity transistor in parallel.

F.4 Current mirror using unity transistors

Most of the current scaling performed in switched current circuits is performed using some sort of current mirror. Even the current copier with an extra current output operates as a current mirror in the copy phase.

Until now we have only considered statistical errors for a single MOS transistor and for a parallel connection of unity transistors. It is however more interesting to investigate the matching error in a current mirror build from unity transistors.

In Fig. F.4 we have a current mirror build from $N + M$ unity transistors and giving a current ratio of

$$m = \frac{i_{OUT}}{i_{IN}} = \frac{i_{11} + i_{12} + \cdots + i_{1M}}{i_{21} + i_{22} + \cdots + i_{2N}} \tag{F.22}$$

the mean current ratio is given by

$$\overline{m} = \frac{M}{N} \tag{F.23}$$

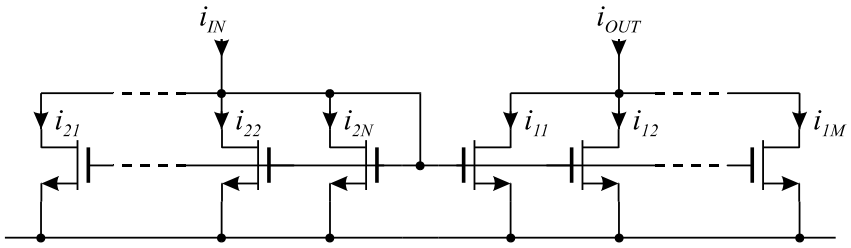

Figure F.4: Current mirror made from unity transistors

and the relative variance of the current ratio is given by

$$\frac{\sigma_m^2}{\overline{m}^2} = \frac{\sigma_{i_{out}}^2}{\overline{i_{out}}^2} + \frac{\sigma_{i_{in}}^2}{\overline{i_{in}}^2} \tag{F.24}$$

$$= \frac{1}{M}\frac{\sigma_{i_o}^2}{\overline{i_o}^2} + \frac{1}{N}\frac{\sigma_{i_o}^2}{\overline{i_o}^2} \tag{F.25}$$

$$= \underline{\frac{\sigma_{i_o}^2}{\overline{i_o}^2}\left(\frac{1}{M} + \frac{1}{N}\right)} \tag{F.26}$$

This equation shows that the accuracy of the current mirror is increased by increasing the number of unity transistors used in the current mirror. This effectively reduces the effect of mismatches in the threshold voltages among the unity transistors, which in turn reduces the nonlinearity of the current mirror.

Part IV

Publications

The following papers have been published as a part of my Ph.D. study.

1. Switched Current Micropower 4th Order Lowpass / Highpass Filter

Presented at:
The Ninetenth European Solid State Circuits Conference ESSCIRC'93
Sevilla–Spain
September 22-24.

2. Generation of a Neuron Transfer Function and its Derivatives

Published in:
Electronics Letters
Volume 29 Number 21
14th October 1993.

3. An Angledetector based on Magnetic Sensing

Presented at:
The International Conference on Circuits and Systems
ISCAS'94
London 30 May - 2 June
Volume 5 of 6
Linear Circuits and Systems
Analog Signal Processing.

4. A Digital Volume Control for Hearing Aid Applications

Presented at:
The Twelfth NORCHIP Seminar
Gothenburg
8 - 9 November 1994.

5. Position Detection with the use of MAGFET's

Presented at:
The Instrumentation/Measurement Technology Conference
IMTC'95
Westin Hotel
Waltham, Massachusetts
April 24-26, 1995.

6. A Neural Flow Estimator

Precented at:
The Instrumentation/Measurement Technology Conference
IMTC'95
Westin Hotel
Waltham, Massachusetts
April 24-26, 1995.

7. A Silicon Potentiometer for Hearing Aids

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