Chapter 2

Design of Current Copiers

In Chapter 1 we introduced the basic building blocks necessary for building SI circuits. We also gave a small example of a switched-current sample delay and found that the simple implementation had some rather large errors.

In this chapter we will focus on how to enhance the operation of current copier circuits. The treatment of this subject will be done in general terms using transconductors and current conveyors as the basic building blocks. We will cover both single ended and fully differential current copier topologies.

2.1 Current Transmission Errors

When we applied a single current pulse at the input of the simple sample delay shown in Chapter 1 the corresponding current pulse at the output of the sample delay was approximately 3% smaller in amplitude than the input pulse.

This error is partly a current transmission error caused by the finite output conductance g_o of the transconductor used in the current copiers and by the feedback capacitance C_F from the transconductor output to the storage capacitor C_S as shown in Fig. 2.1.

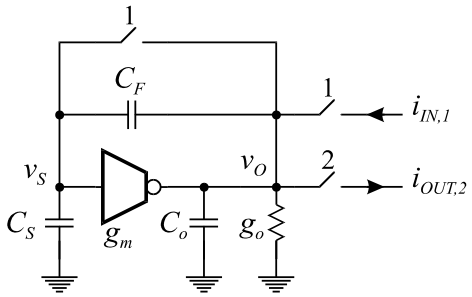

Figure 2.1: Basic current copier including its parasitics

In Appendix B and Appendix C, thorough analysis of the current transmission errors encountered in SI circuits have been made, and it was found that there are basically two ways to reducing these errors as summarized below.

1. Decrease the output conductance g_o and the feedback capacitance C_F.

2. Reduce any signal dependent voltage variations v_O at the output of the transconductor. This will prevent any error currents from flowing in the finite output conductance g_o and

it will also prevent any error charges from entering the storage capacitor C_S through the feedback capacitor C_F. This can be arranged by increasing the input conductance g_m of the current copier or of the current mirror to which the current copier is connected.

In the following subsections we will illustrate how the simple current copier shown in Fig. 2.1 can be enhanced according to the previously summarized techniques.

2.1.1 Decrease of output conductance and feedback capacitance

The output conductance and the feedback capacitance of a transconductor can be decreased by passing the output current of the transconductor through a current conveyor as shown in Fig. 2.2. The current conveyor (CCII−) effectively isolates any voltage variations at the output of the current copier from the output of the transconductor. At the same time we notice that the current conveyor actually operates as a cascoding of the transconductor [21][22] effectively decreasing the output conductance g_z to a small value.

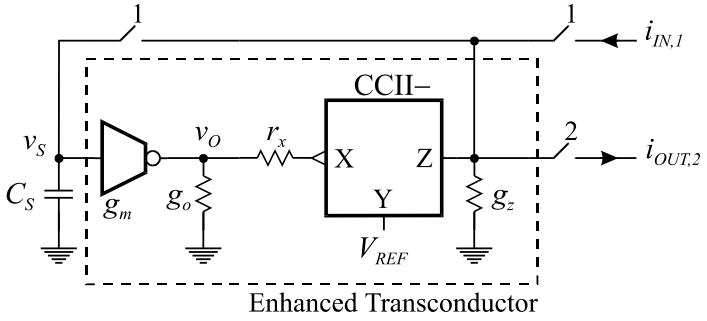

Figure 2.2: Cascode

In practical circuits the current conveyor can not be made ideal. This implies that there will be a small signal transmission from the Z node back to the X node. In order to reduce the effect of this even further we can insert an inverting amplifier between the output node of the transconductor and the Y terminal of the current conveyor. This arrangement is shown in Fig. 2.3. We notice that this circuit is effectively a regulated cascode [23][21] of the transconductor, decreasing the output conductance g_z and isolating the voltage variations even further.

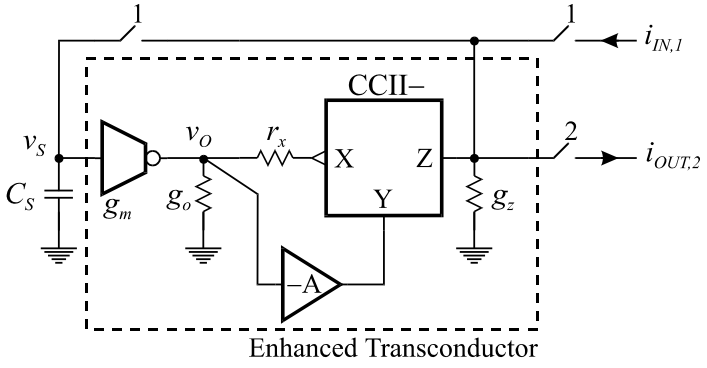

Figure 2.3: Regulated cascode

In the circuits shown in Fig. 2.2 and Fig. 2.3 the resistance r_x represents the input resistance of the X input.

2.1.2 Increase of input conductance

The input conductance of the current copier can be increased by inserting the transconductor in a feedback loop as shown in Fig. 2.4. In the copy phase i.e. phase 1, the current conveyor

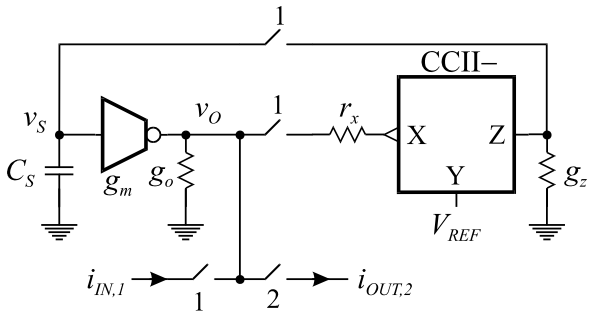

Figure 2.4: Cascode II

(CCII−) and the transconductor are in a closed feedback loop, effectively increasing the input conductance to

$$y_{in} = g_o + g_x \left(1 + \frac{g_m}{g_z}\right)$$

In the hold phase i.e. phase 2, the current conveyor is released from the transconductor and the transconductor can now deliver the stored current at the output. The output conductance is now

$$y_{out} = g_o$$

Based on the results in Appendix B and Appendix C we can now estimate the current transmission error to be approximately

$$\epsilon \simeq 2\frac{y_{out}}{y_{in}} = 2\frac{g_o}{g_o + g_x\left(1 + \frac{g_m}{g_z}\right)}$$

2.2 Single ended Current Copiers and Current Mirrors

This section will show how we systematically can derive many of the already published current copier circuits [24][25][16][26][9][20] , using the enhancement techniques, for reducing current transmission errors, described in the previous section.

2.2.1 Simple

Referring to Fig. 2.1 we see that the simplest current copier can be designed by implementing the transconductor with a single MOS transistor. Such a realization is shown in Fig. 2.5. In this figure the storage capacitor is the gate-source capacitor C_{GS1} and the feedback capacitor is the gate-drain capacitor C_{GD1}. The transconductor output conductance is the output conductance $g_{o1} + g_{o2}$. The transistor $M4$ operates as a current source.

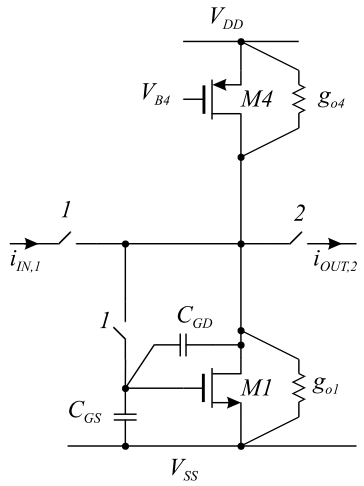

Figure 2.5: Simple Current Copier

Based on the results found in Appendix B and Appendix C we can now write the current transmission error as

$$\epsilon \simeq 2\frac{g_{o1}+g_{o2}}{g_{m1}} + \frac{C_{GD1}}{C_{GD1}+C_{GS1}} \tag{2.1}$$

$$\simeq 4\frac{g_{o1}}{g_{m1}} + \frac{C_{GD1}}{C_{GS1}} \tag{2.2}$$

For a MOS transistor operating in saturation we have that

$$C_{GS} = \frac{2}{3}C'_{OX}WL \tag{2.3}$$

$$C_{GD} = C'_{OX}WL_D \tag{2.4}$$

if we insert these equations into (2.2) we get that the current transmission error is given by

$$\underline{\epsilon \simeq 4\frac{g_{o1}}{g_{m1}} + \frac{3}{2}\cdot\frac{L_D}{L}} \tag{2.5}$$

Example 2.2.1
For a MOS transistor it is reasonable to assume that the intrinsic gain $A_i = g_m/g_o$ is in the order of $g_m/g_o \simeq 100$. We will also assume that $L \simeq 30\mu m$ and $L_D \simeq 0.3\mu m$.

If we insert these values into (2.5) we get that the current transmission error is in the order of magnitude of

$$\epsilon \simeq 4\frac{1}{100} + \frac{3}{2}\cdot\frac{0.3}{30} \sim 5.5\% \tag{2.6}$$

This is indeed a large error that will result in a gain of the current copier of 0.95. For most practical purposes this error is far to large. ■

2.2.2 Cascode

Referring to Fig. 2.2 we saw that the current transmission error could be reduced by connecting a current conveyor (CCII−) to the output of the transconductor. By implementing the transconductor and the current conveyor as single NMOS transistors [25] we get the circuit

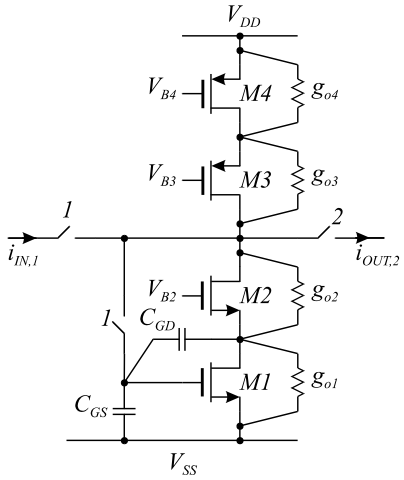

Figure 2.6: Cascode Current Copier

shown in Fig. 2.6. In this figure the transistor M1 is the transconductor, M2 operates as the current conveyor and the transistor M3 and M4 operate as a cascode current sources.

The cascoding transistor M2 (Current Conveyor) has the effect of decreasing the effective output conductance of M2 to

$$g_o = \frac{g_{o2}}{1 + \frac{g_{m2}}{g_{o1}}} \tag{2.7}$$

therefore the voltage variations at the output of the current copier to the drain-voltage of M1 (output voltage of the transconductor) are reduced by

$$\frac{v_{D1}}{v_o} = \frac{g_{o2}}{g_{o1}\left(1 + \frac{g_{m2}}{g_{o1}}\right)} \tag{2.8}$$

$$= \frac{g_{o2}}{g_{o1} + g_{m2}} \tag{2.9}$$

$$\simeq \frac{g_{o2}}{g_{m2}} = \frac{1}{A_{i2}} \tag{2.10}$$

which is the intrinsic gain of the cascoding transistor M2. The reason for using a cascode current source, M3 and M4, is that the output conductance of the current source must be in the same order of magnitude as the effective output conductance of the cascode transistor M2 in order to not being the dominating output conductance.

Because the voltage variations at the output of the transconductor M1 have been reduced by a factor given by (2.10) the current transmission error is reduced by the same amount. Combining this fact with (2.5) we get that the current transmission error is reduced to

$$\underline{\epsilon \simeq \frac{g_{o2}}{g_{m2}}\left(4\frac{g_{o1}}{g_{m1}} + \frac{3}{2}\cdot\frac{L_D}{L}\right)} \tag{2.11}$$

Example 2.2.2
For a MOS transistor it is reasonable to assume that the intrinsic gain $A_i = g_m/g_o$ is in the order of $g_m/g_o \simeq 100$. We will also assume that $L \simeq 30\mu m$ and $L_D \simeq 0.3\mu m$.

If we insert these values into (2.11) we get that the current transmission error is in the order of magnitude of

$$\epsilon \simeq \frac{1}{100}\left(4\frac{1}{100} + \frac{3}{2}\cdot\frac{0.3}{30}\right) \sim 0.06\% \tag{2.12}$$

This is a reasonably small error that will result in a gain of the current copier of 0.9995. For most practical purposes this is tolerable. ■

2.2.3 Folded Cascode

The current copier shown in Fig. 2.6 was derived from the assumption that the transconductor and the current conveyor were both implemented using a single NMOS transistor. If we however implement the current conveyor as a single PMOS transistor we get a folded cascode current copier as shown in Fig. 2.7. This circuit is basically the same as shown in Fig. 2.6

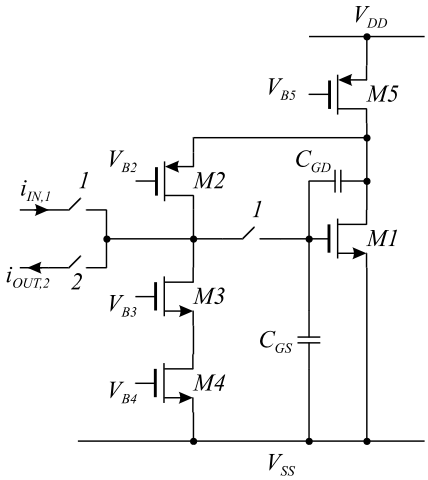

Figure 2.7: Folded Cascode Current Copier

except that the cascode has been folded.

The performance of the folded cascode current copier shown in Fig. 2.7 is the same as the performance of the traditionally cascode current copier shown in Fig. 2.6

2.2.4 Regulated Cascode

We have previously seen that the current transmission error could by cascoding, be reduced to something in the order of 0.06%. This is in most cases a tolerable error, but in some cases we might want the error reduced even further. This can be accomplished by using double cascoding or even higher cascoding [22]. Another possibility is to use regulated cascode arrangement [23] which gives a performance comparable to double cascoding.

A current copier utilizing regulated cascoding is shown in Fig. 2.8. This circuits is based on Fig. 2.3, where the transconductor is implemented using a single NMOS transistor M1. The current conveyor is implemented as M2 and the inverting amplifier is implemented by M5.

The current transmission error can be found by the following reasoning: Assuming that we have made a cut in the loop formed by M2 and M5, we get that the effective output conductance of M2 is given by (2.7). The loop gain around the cut that we have made is given by

$$L_{Gain}^{Cut} = \frac{g_{m5}}{g_{o5} + g_{o8}} \tag{2.13}$$

When we close the loop (no cut) the effective output conductance of M2 is decreased by the

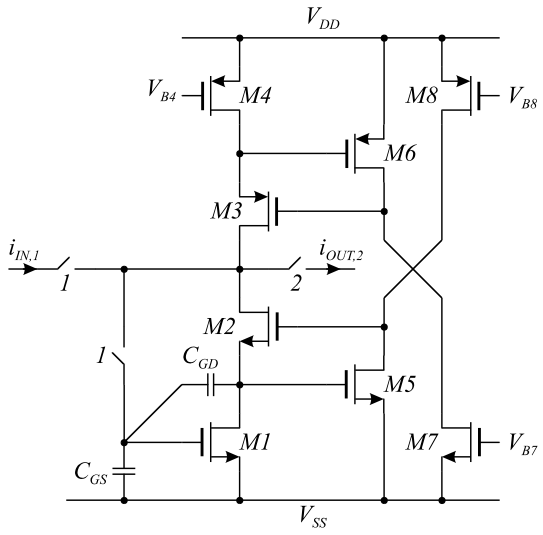

Figure 2.8: Regulated Cascode Current Conveyor

loop-gain L_{Gain}^{Cut} giving a output conductance of

$$g_o = \frac{g_{o2}}{1+\frac{g_{m2}}{g_{o1}}} \cdot \frac{g_{o5}+g_{o8}}{g_{m5}} \tag{2.14}$$

therefore the voltage variations from v_O to the drain-voltage of M1 (output voltage of the transconductor) are reduced by

$$\frac{v_{D1}}{v_o} = \frac{g_{o2}}{g_{o1}\left(1+\frac{g_{m2}}{g_{o1}}\right)} \cdot \frac{g_{o5}+g_{o8}}{g_{m5}} \tag{2.15}$$

$$= \frac{g_{o2}}{g_{o1}+g_{m2}} \cdot \frac{g_{o5}+g_{o8}}{g_{m5}} \tag{2.16}$$

$$\simeq \frac{g_{o2}}{g_{m2}} \cdot \frac{2g_{o5}}{g_{m5}} = \frac{1}{A_{i2}} \cdot \frac{2}{A_{i5}} \tag{2.17}$$

which is the intrinsic gain of the cascoding transistor M2 and the amplifier M5.

Because the voltage variations at the output of the transconductor, M1, have been reduced by a factor given by (2.17) the current transmission error is reduced by the same amount. Combining this fact with (2.5) we get that the current transmission error is reduced to

$$\underline{\epsilon \simeq \frac{g_{o2}}{g_{m2}} \cdot \frac{2g_{o5}}{g_{m5}} \left(4\frac{g_{o1}}{g_{m1}} + \frac{3}{2} \cdot \frac{L_D}{L}\right)} \tag{2.18}$$

Example 2.2.3
For a MOS transistor it is reasonable to assume that the intrinsic gain $A_i = g_m/g_o$ is in the order of $g_m/g_o \simeq 100$. We will also assume that $L \simeq 30\mu m$ and $L_D \simeq 0.3\mu m$.

If we insert these values into (2.18) we get that the current transmission error is in the order of magnitude of

$$\epsilon \simeq \frac{1}{100} \cdot \frac{2}{100}\left(4\frac{1}{100} + \frac{3}{2} \cdot \frac{0.3}{30}\right) \sim 0.001\% \tag{2.19}$$

This is indeed a very small error that will result in a gain of the current copier of 0.99999. ■

2.2.5 Regulated Folded Cascode

The current copier shown in Fig. 2.8 was derived from the assumption that the transconductor and the current conveyor were both implemented using single NMOS transistor. If we however implement the current conveyor as a single PMOS transistor we get a folded regulated cascode current copier as shown in Fig. 2.9. This circuits is basically the same as shown in Fig. 2.8

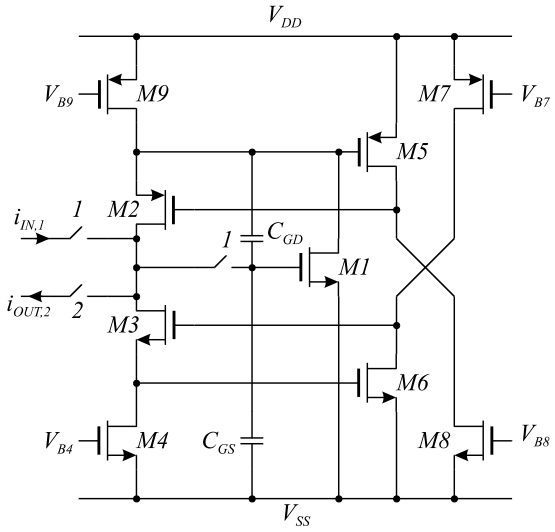

Figure 2.9: Regulated Folded Cascode Current Copier

except that the cascode has been folded.

The performance of the folded regulated cascode current copier shown in Fig. 2.9 is the same as the performance of the regulated cascode current copier shown in Fig. 2.8

2.2.6 Cascode II

Referring to Fig. 2.4 we saw that the current transmission error could be reduced by connecting the transconductor in a feedback loop with a current conveyor (CCII−) in the copy phase. The effect of this feedback was to increase the input conductance in the copy phase and thereby reduce the current transmission error. By implementing the transconductor as a single NMOS transistor and the current conveyor as a PMOS transistor we get the circuit shown in Fig. 2.10. In this figure the storage capacitor is the gate-source capacitor C_{GS1} and the feedback capacitor is the gate-drain capacitor C_{GD1}. The transconductor output conductance is the output conductance $g_{o1} + g_{o5}$. The transistor M2 operates as the current conveyor and the transistor M3 and M4 operate as a cascode current source.

The output conductance in the copy phase of the current copier can be found by the following reasoning: Assuming that we cut the loop formed by M1 and M2 we get that the output conductance is given by

$$g_o = g_{o1} + g_{o5} + g_{o6} + g_{m2} \tag{2.20}$$

The loop-gain around the cut is given by

$$L_{Gain}^{Cut} = g_{m1} \frac{g_{m2}}{g_{o1} + g_{o5} + g_{o6} + g_{m2}} \cdot \frac{1 + \frac{g_{m3}}{g_{o4}}}{g_{o3}} \tag{2.21}$$

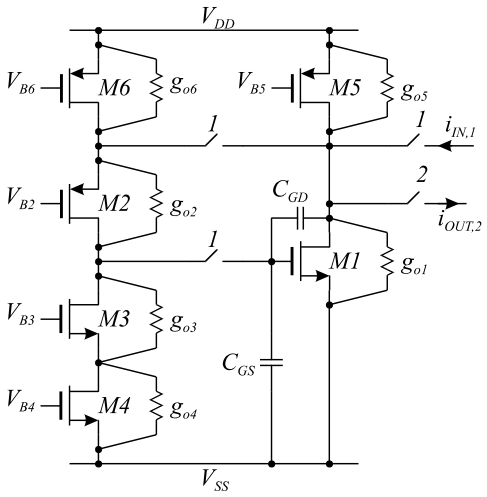

Figure 2.10: Cascode II Current Copier

When we close the loop by removing the cut, the input conductance will increase to

$$g_o = (g_{o1} + g_{o5} + g_{o6} + g_{m2}) \left(1 + g_{m1} \frac{g_{m2}}{g_{o1} + g_{o5} + g_{o6} + g_{m2}} \cdot \frac{1 + \frac{g_{m3}}{g_{o4}}}{g_{o3}}\right) \tag{2.22}$$

$$= (g_{o1} + g_{o5} + g_{o6} + g_{m2}) + g_{m2} \left(1 + g_{m1} \frac{1 + \frac{g_{m3}}{g_{o4}}}{g_{o3}}\right) \tag{2.23}$$

By using this arrangement with the current copier, the voltage swing at the output of the transconductor has been decreased to

$$\frac{g_{m1}}{(g_{o1} + g_{o5} + g_{o6} + g_{m2}) + g_{m2} \left(1 + g_{m1} \frac{1 + \frac{g_{m3}}{g_{o4}}}{g_{o3}}\right)} \tag{2.24}$$

$$\simeq \frac{g_{o3}}{g_{m3}} \cdot \frac{g_{o4}}{g_{m2}} \tag{2.25}$$

Because the voltage variations at the output of the transconductor, M1, have been reduced by a factor given by (2.25) the current transmission error is reduced by the same factor. Combining this fact with (2.5) we get that the current transmission error is reduced to

$$\underline{\epsilon \simeq \frac{g_{o3}}{g_{m3}} \cdot \frac{g_{o4}}{g_{m2}} \left(4 \frac{g_{o1}}{g_{m1}} + \frac{3}{2} \cdot \frac{L_D}{L}\right)} \tag{2.26}$$

Example 2.2.4
For a MOS circuits it is reasonable to assume that the intrinsic gain $A_i = g_m/g_o$ is in the order of $g_m/g_o \simeq 100$. We will also assume that $L \simeq 30\mu m$ and $L_D \simeq 0.3\mu m$.

If we insert these values into (2.26) we get that the current transmission error is in the order of magnitude of

$$\epsilon \simeq \frac{1}{100} \cdot \frac{1}{100} \left(4 \frac{1}{100} + \frac{3}{2} \cdot \frac{0.3}{30}\right) \sim 0.0006\% \tag{2.27}$$

This is indeed a very small error that will result in a gain of the current copier of 0.999995. ■

Class AB

All of the current copier cells described so far have all operated in class A. This implies that the signal current can not exceed the quiescent currents used for biasing the cells.

In order to overcome this we have to ensure that the current copier cell is capable of operating in class AB. This can be done by using class AB transconductors. One example of a class AB, Cascode II current copier is shown in Fig. 2.11.

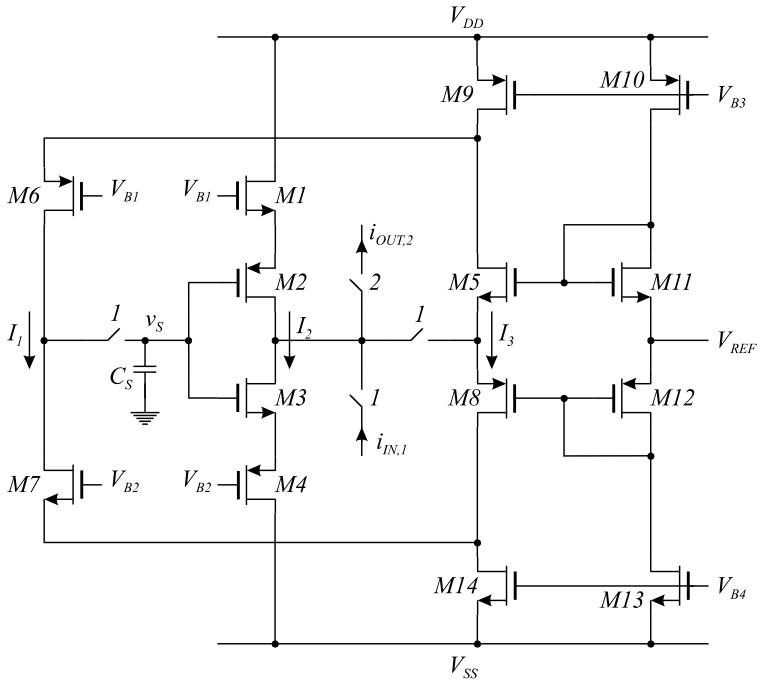

Figure 2.11: Class AB, Cascode II Current Copier

This current copier is fully symmetrical which of course will make it more linear than the previously described current copiers. At the same time it is capable of handling signal currents somewhat larger than the quiescent current.

The transconductor is a class AB design using compound MOS transistors (Appendix A), made from M1,M2,M3 and M4. The reason for using compound MOS transistors in this transconductor is that they isolate any voltage variations on the supply voltages from the storage capacitor C_S. In fact if we did not care about the effect of these voltage variations we could simply have used a CMOS inverter as a transconductor (M2 and M3) and removed M1 and M4.

The storage capacitor shown as the separate capacitor C_S in Fig. 2.11 could be the combination of gate-source capacitors for M1,M2,M3 and M4.

The current conveyor (CCII−) is made from the transistors M5,M6,M7 and M8, which gives a fully symmetrical current conveyor. The rest of the circuitry is for biasing and can be shared by other current copier cells.

2.3 Differential Current Copiers and Current Mirrors

Very often, fully differential circuit configurations are used in high performance analog circuit designs. This of course also applies to switched-current circuits, where fully differential

designs will reduce the effect of clock feedthrough and charge injection considerably [24]. Also fully differential designs have a much better power supply rejection.

2.3.1 Simple

A fully differential current copier can easily be build using a MOS differential pair as a transconductor [24], such an arrangement is shown in Fig. 2.12.

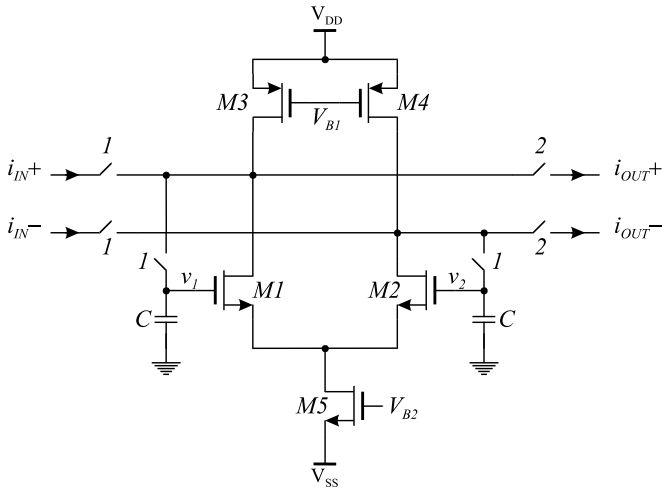

Figure 2.12: Simple Fully Differential Current Copier

The performance of this current copier will be rather limited as the performance of the simple single ended current copier shown in Fig. 2.5. One major source of errors in this design is the current transmission errors.

In order to get this current copier to operate we also have to introduce some commonmode regulation that can regulate the commonmode voltage $(v_1+v_2)/2$ to a well known value. This can be done in several ways e.g. by controlling the current in transistors M3 and M4 or by controlling the tail current in M5.

In order to build useful fully differential SI circuits, we have to enhance the simple current copier shown in Fig. 2.12. We can do so using the same techniques as described in the beginning of this chapter, where we showed a topology that decreases the output conductance of the current copier leading to a cascode structure, and a topology that increases the input conductance leading to the Cascode II structure. These two techniques will be illustrated in the following section.

2.3.2 Cascode and Cascode II

In the beginning of this chapter we showed that the output conductance of the simple current copier could be decreased by using the topology shown in Fig. 2.2 and we showed that the input conductance could be increased by using the topology shown in Fig. 2.4

In order to adapt these topologies to our fully differential designs we have to construct a fully differential current conveyor (CCII−) including a commonmode regulation. In Fig. 2.13 and Fig. 2.14 we have shown how the fully differential current conveyor should be connected to the differential pair in order to construct the cascode and the cascode II current copiers. The actual implementation of the fully differential current conveyor and the commonmode regulation is not shown in these figures, but will be shown in a forthcoming section. We

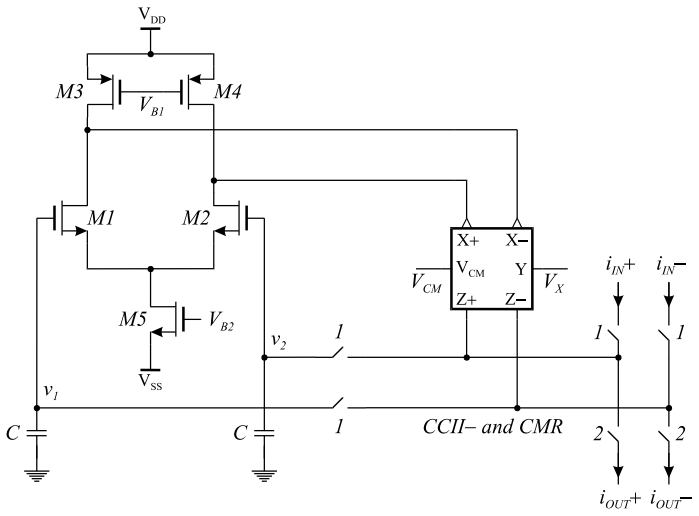

Figure 2.13: Fully Differential Cascode Current Copier

have however shown that the CCII− needs two external bias voltages shown as V_{CM} and V_X. Here V_{CM} is the desired commonmode voltage $(v_1 + v_2)/2$ and V_X is the voltage that is to put on the $X+$ and $X-$ inputs.

The storage capacitors, shown as the capacitors C, in Fig. 2.13 and Fig. 2.14, could be the gate-source capacitors of the transistors M1 and M2 in the MOS differential pair (transconductor) or they could be some separate MOS capacitors.

In case there is a need for rather large storage capacitors, e.g. in low noise circuits, it can be advantageous to use separate MOS capacitors because large gate-source capacitors lead to large parasitic drain capacitors that could introduce some ringing in the settling behavior of the current copier, this is discussed in detail in Appendix C.

By looking at the fully differential current copiers shown in Fig. 2.13 and Fig. 2.14 we notice that they are relatively complicated circuits that could be hard to justify just to get a simple current copier functionality.

However we have to consider the fact that we seldomly need a single stand alone current copier, but a combination of current copiers that make up a SI building block such as a sample delay a integrator or a differentiator. In that case the current conveyor can be shared between the current copiers and the circuit becomes somewhat simpler, this technique is described in detail in Chapter 3.

2.3.3 Fully Differential Current Conveyors and Commonmode Regulation

In this section we will show three alternative implementations of fully differential current conveyors, including commonmode regulations.

All of the current conveyors are based on a foldet cascode topology as can be seen from Fig. 2.15, Fig. 2.16 and Fig. 2.17. In these figures the transistors M3 and M4 operate as the actual current conveyors and the transistors M1,M2,M5,M6,M7 and M8 operate as current sources.

The current conveyor and commonmode regulation shown in Fig. 2.15 is often used in conjunction with fully differential foldet cascode transconductors (OTA's) [27]. From Fig. 2.13 we see that the differential pair together with the current conveyor shown in Fig. 2.15 is such a foldet cascode transconductor.

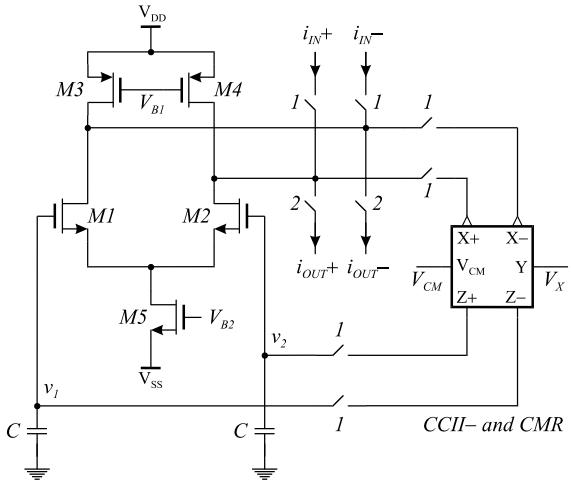

Figure 2.14: Fully Differential Cascode II Current Copier

The commonmode regulation used in the current conveyor in Fig. 2.15 is based on a resistor degenerated current source. The commonmode regulation operates in the following manner: The transistors M9 and M10 are biased in their linear region where they effectively operate as voltage controlled resistors that degenerate the current source made from M7 and M9. The effective conductance used for degeneration is the sum of the conductance of M9 and M10. The conductance of M9 will vary linearily with the voltage at $Z+$ and the conductance of M10 will vary linearily with the voltage at $Z-$, therefore the sum of the conductances will only depend on the sum of the voltages at $Z+$ and $Z-$ i.e. the commonmode voltage at the Z output.

The commonmode regulation used in the current conveyor in Fig. 2.16 is based on two differential pairs M11,M12 and M13,M14. It is easily seen that the commonmode regulation current i_{CMR} is only dependent on the commonmode voltage at the Z output and not on the differential voltage.

The commonmode regulation current is used to control the bias current in the transistors M1 and M2. When the commonmode voltage at the Z output increases the current i_{CMR} decreases which in turn decreases the current flowing through M1 and M2. This effectively forces the commonmode voltage back to its fixed value.

The commonmode regulation used in the current conveyor in Fig. 2.17 is somewhat similar in operation to the commonmode regulation used in Fig. 2.16. The operation of this commonmode regulation is as follows: The transisors M15 and M17 form a differential pair that senses the voltage at the Z output. The source voltage of this differential pair is almost independent of the differential voltage whereas it is strongly dependent on the commonmode voltage (see Appendix A). When the commonmode voltage at the Z output increases the source voltage of the differential pair M15,M17 increases which in turn decreases the current i_{CMR} and the commonmode voltage is forced back to its fixed value.

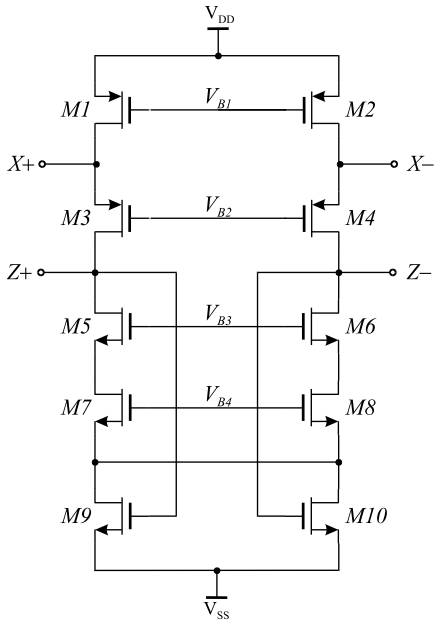

Figure 2.15: Fully differential CCII– including a commonmode regulation based on resistor degeneration

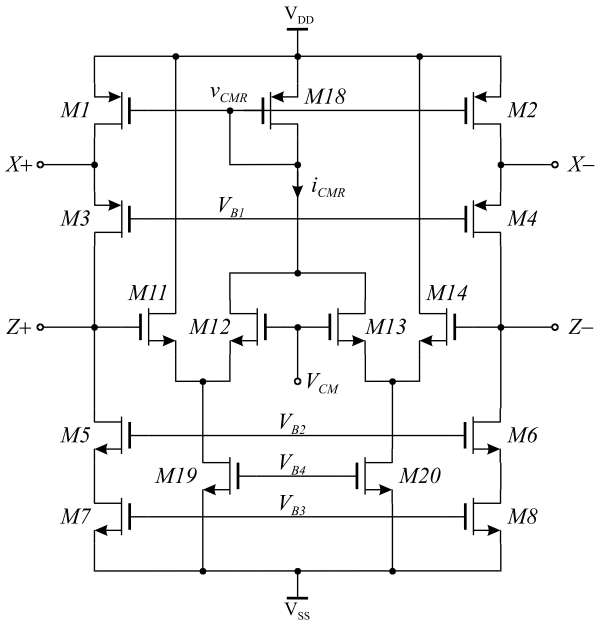

Figure 2.16: Fully differential CCII– including a commonmode regulation based on current steering

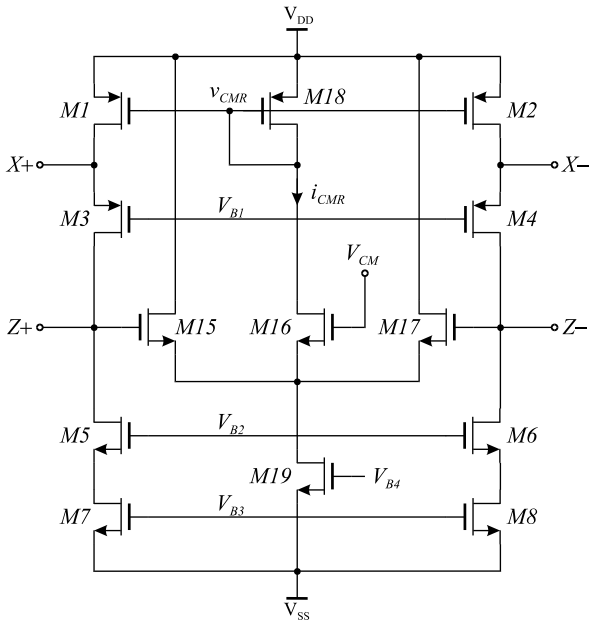

Figure 2.17: Fully differential CCII– including a commonmode regulation based on current steering