Chapter 3

Design of Switched Current Building Blocks

In this chapter we show how current copiers can be used in the design of many of the most fundamental SI building blocks. The building blocks described in this chapter are; Sample delays, Delay lines, Integrators and Differentiators.

We also discuss how current transmission errors limit the performance of the building blocks.

3.1 Sample Delays

The sample delay is one of the fundamental signal processing operations in digital signal processing circuits and in analog sampled data systems. It is therefore very interesting to know how to build sample delays using switched current circuits, because it is the backbone in many of our building blocks e.g. the integrator.

We have previously seen that the current copier, in itself, is an inverting delay of a half clock period i.e. its transfer function can be described as

$$H(z) = -z^{-1/2} \tag{3.1}$$

A sample delay i.e. a delay of one clock period has a transfer function given by

$$H(z) = z^{-1} \tag{3.2}$$

From the above equations it is therefore obvious that a sample delay is naturally constructed by cascading two current copiers as shown in Fig. 3.1. From the SFG in Fig. 3.1 we see that the overall transfer function formed by the cascading of two current copiers is given by

$$H(z) = (-z^{-1/2}) \cdot (-z^{-1/2}) = z^{-1} \tag{3.3}$$

which is a sample delay as expected.

In Appendix C and in Chapter 2 we have shown that all current copiers have some degree of current loss. The effect of this current loss is that the output current from the CCOP is slightly smaller than the input current. The effect of this, on SI building blocks, is easily taken into account by replacing the ideal CCOP transfer function

$$H(z) = -z^{-1/2} \tag{3.4}$$

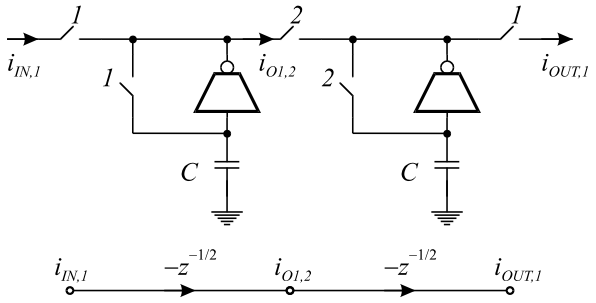

Figure 3.1: Sample Delay made from cascading of two current copiers

with the modified transfer function

$$H(z) = -(1-\epsilon)z^{-1/2} \tag{3.5}$$

where ϵ denotes that current transmission loss.

The transfer function of the sample delay, taking into account the current loss, is now given by

$$H(z) = (-(1-\epsilon)z^{-1/2}) \cdot (-(1-\epsilon)z^{-1/2}) = (1-\epsilon)^2 z^{-1} \simeq (1-2\epsilon)z^{-1} \tag{3.6}$$

This equation shows that the sample delay will have almost twice the current loss of a single CCOP.

The topology of the sample delay shown in Fig. 3.1 applies to all of the Cascode current copiers described in the previous chapter with the exception of the Cascode II CCOP, this is easily seen if we replace the transconductors in Fig. 3.1 by the transconductors used in Fig. 2.2 and Fig. 2.3 that have been enhanced by current conveyors.

A sample delay made from the Cascode II structure is shown in Fig. 3.2. This sample

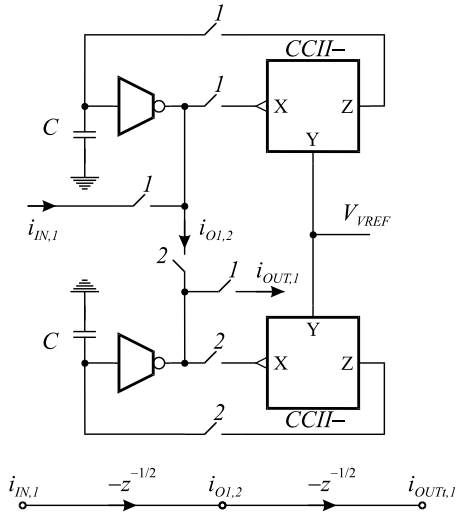

Figure 3.2: Sample Delay made from cascading of two Cascode II current copiers

delay might look a little bit complicated because it contains two current conveyors, but we notice that the two current conveyors (CCII−) operate on opposite clock phases and can

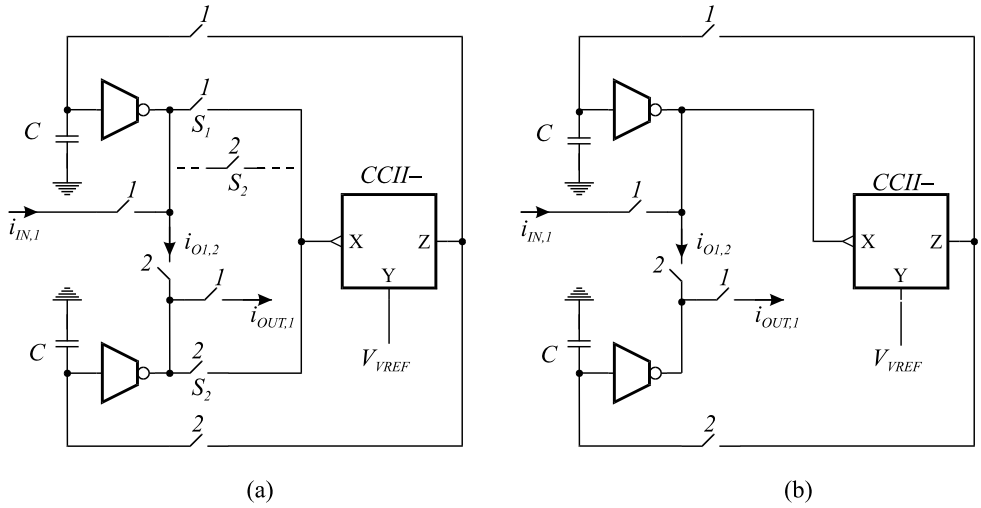

Figure 3.3: (a) Simplified Delay made from cascading of two Cascode II CCOP's; (b) Final Sample Delay made from cascading of Cascode II CCOP's

therefore be replaced by a single current conveyor that is shared by the two transconductors, as shown in Fig. 3.3 (a).

By investigating this figure we see that it is possible to move the switch S_2 so that it is in parallel with the switch S_1 (shown as the dashed switch) without altering the functionality of the circuit. The two switches S_1 and S_2 that now are in parallel operate on opposite clock phases, the effect of this is that these two switches can be replaced by a short circuit, which leads us directly to the circuit shown in Fig. 3.3 (b).

To illustrate how the sample delay shown in Fig. 3.3 (b) can be implemented, we have made two examples as shown in Fig. 3.4. In both examples the transconductors are imple-

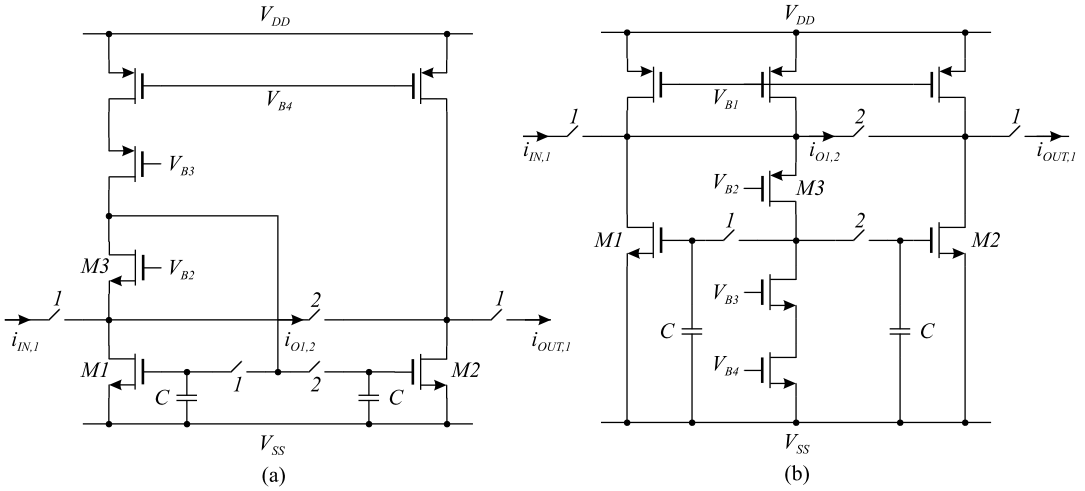

Figure 3.4: (a) Cascode implementation of sample delay; (b) Folded Cascode implementation of sample delay

mented as single NMOS transistors M1 and M2. In the first example (a) the current conveyor (M3) is implemented using a NMOS transistor and in the second example (b) the current

conveyor (M3) is implemented using a PMOS transistor.

The storage capacitor shown as C can be the gate-source capacitor of the transistors M1 and M2.

3.2 Delay Lines

An other rather important building block in digital signal processing circuits and in analog sampled data systems is the delay line. The delay line is for instance a fundamental building block in FIR filters. It is therefore very interesting to know how to build delay lines in switched current circuits,

3.2.1 Cascade

The most obvious way to construct a delay line is to cascade several sample delays. Such an arrangement is shown in Fig. 3.5. The transfer function from the input to the N'th output

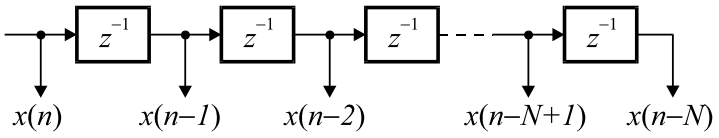

Figure 3.5: Delay Line made from cascoding of sample delays

is given by

$$H_N(z) = (z^{-1})^N = z^{-N} \tag{3.7}$$

If we however take into account the current loss found in each sample delay we get that the overall transfer function of the delay line is given by

$$H_N(z) = ((1-\epsilon)^2 z^{-1})^N = (1-\epsilon)^{2N} z^{-N} \simeq (1-2N\epsilon) z^{-N} \tag{3.8}$$

One advantage of this concept is that it is relatively easy to get tapped outputs from the delay line by simply adding some extra output transconductor to the current copiers used for building the sample delays. In this way it is relatively easy to construct a FIR filter, simply by adding together the extra current outputs of the tapped delay line.

There is however one drawback with this delay line which is that the signal entering the delay line has to travel through several sample delays before it leaves the delay line. This, of course, will deteriorate the signal and introduce distortion and noise.

3.2.2 Polyphase

One way of overcoming the limitations of the cascade delay line, is to introduce a new non-overlapping clock phase for each sample delay and then make use of the topology shown in Fig. 3.6. In the polyphase delay line, each current copier holds a signal sample for N clock periods in contrast to the cascade delay line, where each current copier only holds a signal sample for one clock period. From Fig. 3.6 we see that the transfer function from the input to the output is given by

$$H_N(z) = -(z^{-1})^N = -z^{-N} \tag{3.9}$$

Because the signal current only passes through a single CCOP the current loss will be limited, and the overall transfer function of this polyphase delay line including current loss is given by

$$H_N(z) = -(1-\epsilon)(z^{-1})^N = -(1-\epsilon) z^{-N} \tag{3.10}$$

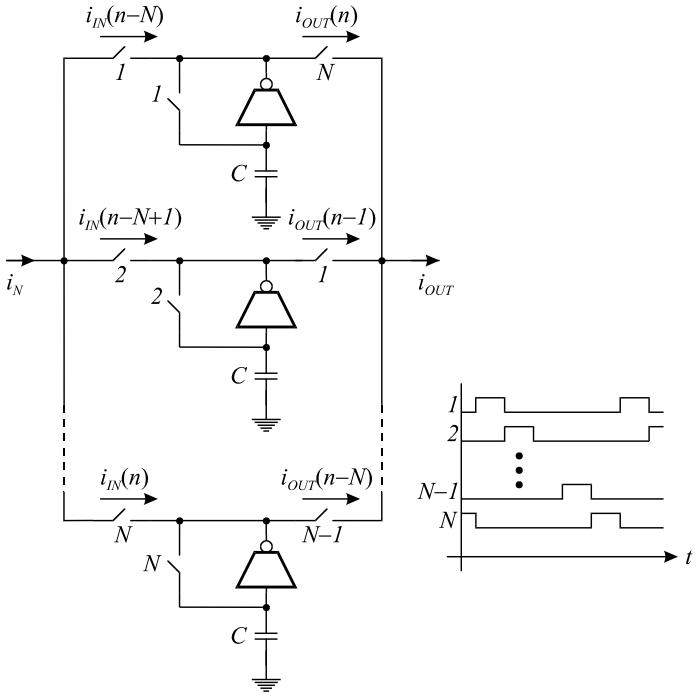

Figure 3.6: Polyphase delay line

3.3 Integrators

The integrator is one of the most widely used building block in all analog signal processing circuits. It is a very versatile component that can be used in the design of almost any filter.

The backbone in the design of integrators is the sample delay. By feeding the output of the sample delay back to its input together with the input signal we get a accumulating effect which is necessary for making an integrator.

3.3.1 Inverting and Non-inverting Integrators

If we take the sample delay shown in Fig. 3.1 and feed the output back to the input together with some external input signal and at the same time add two extra output transconductors to the current copiers in the sample delay, we get the integrator shown in Fig. 3.7 (a). The two output transconductors have optional scaling factors a and b that are used to control the gain of the integrator outputs.

By investigating the integrator shown in Fig. 3.7 (a) we see that the switch S_2 and S_3 are operating on opposite clock phases. Also we notice that the switch S_3 is logically in parallel with the switch S_2 therefore these two switches can be replaced by a short circuit. This leads us directly to the simplified integrator shown in Fig. 3.7 (b).

A signal flow graph SFG, representing the integrator in Fig. 3.7 (a), is shown in Fig. 3.8. From this SFG the transfer functions, from the input $i_{IN,1}$ to the inverting output $i_{OUT1,1}$ and the non-inverting output $i_{OUT2,1}$ is now easily calculated. Using Masons formula we get that the two transfer functions are given by

$$H_{Inv}(z) = \frac{I_{out,1}}{I_{in,1}} = -\frac{a}{1-z^{-1}} \tag{3.11}$$

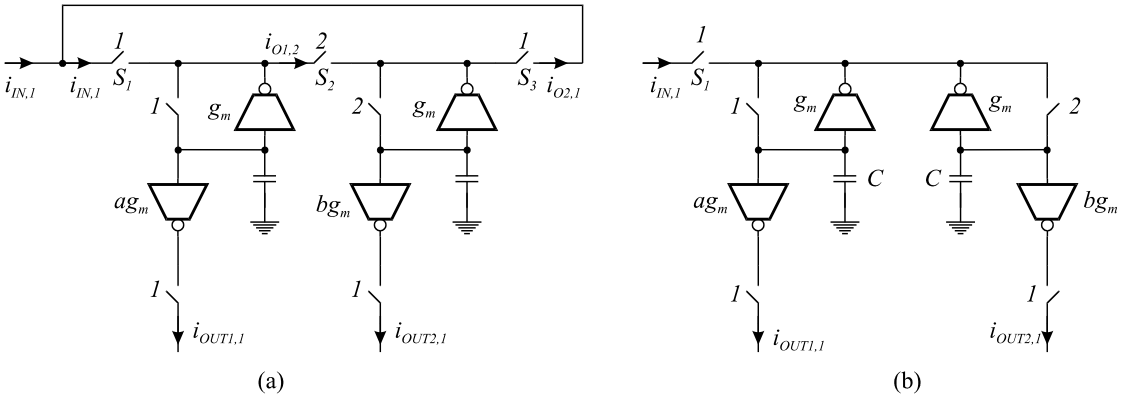

Figure 3.7: (a) Inverting and Noninverting Integrator; (b) Simplified Integrator

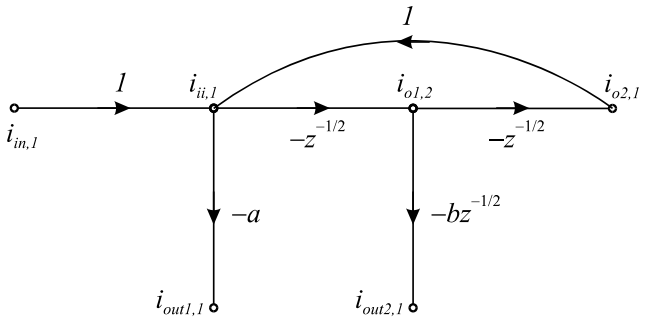

Figure 3.8: SFG for the Inverting and Noniverting Integrator

$$H_{Noninv}(z) = \frac{I_{out,2}}{I_{in,1}} = \frac{bz^{-1}}{1 - z^{-1}} \tag{3.12}$$

If we take into account the effect of the current transmission error we get the following transfer function for the integrator.

$$H_{Inv}(z) = \frac{I_{out,1}}{I_{in,1}} = -\frac{a}{1 - (1-\epsilon)^2 z^{-1}} \simeq -\frac{a}{1 - (1-2\epsilon)z^{-1}} \tag{3.13}$$

$$H_{Noninv}(z) = \frac{I_{out,2}}{I_{in,1}} = \frac{b(1-\epsilon)z^{-1}}{1 - (1-\epsilon)^2 z^{-1}} \simeq \frac{b(1-\epsilon)z^{-1}}{1 - (1-2\epsilon)z^{-1}} \tag{3.14}$$

The ideal integrator has a DC-gain of ∞ but because of the current loss the DC-gain will be limited to some finite value. The DC-gain of the integrator can be found by setting $z = 1$ in the transfer function. If we do so we get that the DC-gain at the two integrator outputs is approximately given by

$$H_{Inv}(z)|_{z=1} \simeq -\frac{a}{2\epsilon} \tag{3.15}$$

$$H_{Noninv}(z)|_{z=1} \simeq \frac{b}{2\epsilon} \tag{3.16}$$

The topology of the integrator shown in Fig. 3.7 applies to all of the Cascode current copiers described in the previous chapter with the exception of the Cascode II CCOP, this is easily seen if we replace the transconductors in Fig. 3.7 by the transconductors used in Fig. 2.2 and Fig. 2.3 that have been enhanced by current conveyors.

A integrator based on Cascode II current copiers can be designed by feeding the output of a Cascode II sample delay, shown in Fig. 3.3 (b), together with an external input signal back to its input and at the same time add two extra output transconductors to the current copiers in the sample delay, we get the integrator shown in Fig. 3.9 (a).

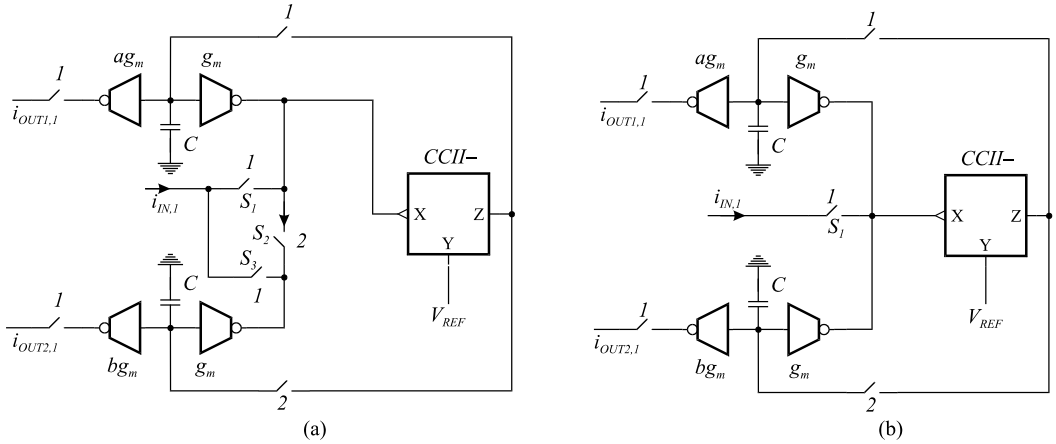

Figure 3.9: (a) Inverting and Noninverting integrator based on Cascode II current copiers; (b) Simplified Inverting and Noninverting integrator based on Cascode II current copiers

By investigating the integrator in Fig. 3.9 we notice that the switches S_2 and S_3 are logically in parallel and operating at opposite clock phases. These switches can therefore be replaced by a short circuit. This leads us directly to the simplified integrator shown in Fig. 3.9 (b).

To illustrate how the integrator shown in Fig. 3.9 (b) can be implemented, we have made two examples as shown in Fig. 3.10. In both examples the transconductors are implemented

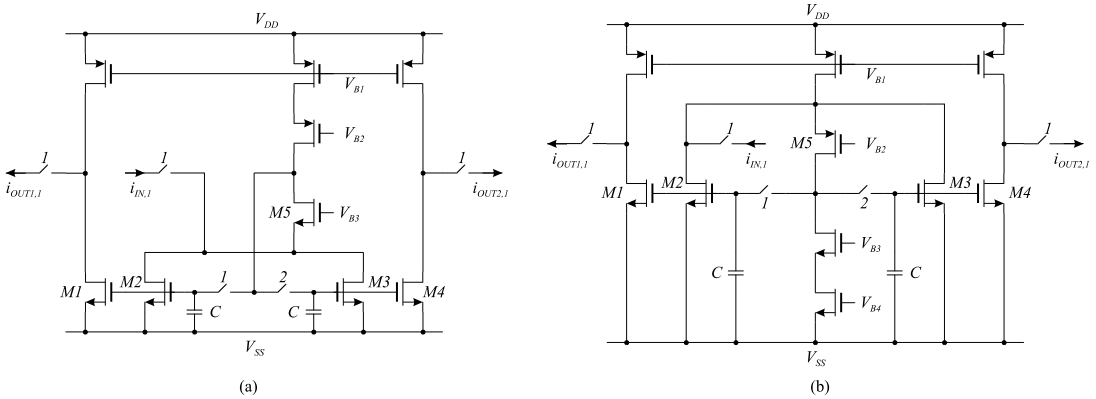

Figure 3.10: (a) Cascode implementation of the integrator; (b) Folded Cascode implementation of the integrator

as single NMOS transistors M1,M2,M3 and M4. In the first example (a) the current conveyor (M5) is implemented using a NMOS transistor and in the second example (b) the current conveyor (M5) is implemented using a PMOS transistor.

3.3.2 Bilinear Integrator

In some situations it might be advantageous to have a bilinear integrator i.e. an integrator with a transfer function given by

$$H(z) = \frac{T}{2} \cdot \frac{1 + z^{-1}}{1 - z^{-1}} \tag{3.17}$$

Such an integrator has the property that the transfer function at half the sampling frequency is zero i.e. $H(z)|_{z=-1} = 0$. The effect of this is that filters based on bilinear integrators often have a desirable zero in their transfer functions at half the sampling frequency.

The easiest way to construct a bilinear SI integrator is to use fully differential SI circuits. An example of a fully differential bilinear integrator is shown in Fig. 3.11.

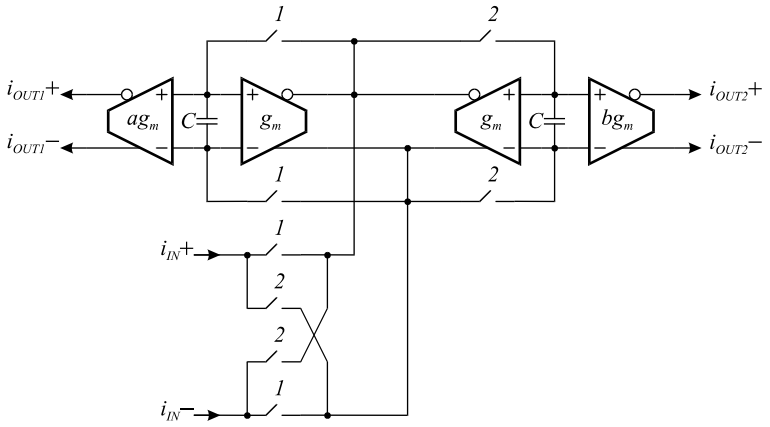

Figure 3.11: Fully differential bilinear integrator

This bilinear integrator has actually two outputs; one bilinear output i_{OUT1} and one ordinary noninverting integrator output i_{OUT2}. The actual transfer functions from the input i_{IN} to the two outputs is given by

$$H_{Bilin}(z) = -a\frac{1 + z^{-1}}{1 - z^{-1}} \tag{3.18}$$

$$H_{Noninv}(z) = 2b\frac{z^{-1}}{1 - z^{-1}} \tag{3.19}$$

The operation of this bilinear integrator is based on the assumption that the input signal current i_{IN} is valid at the input on both clock phase 1 and 2. In a similar way the output current at the bilinear output is also valid on both clock phase 1 and 2. Because of this cascading of bilinear integrators is possible.

In practical circuit designs it is however not desirable to cascade bilinear integrators because the signal currents have to settle throughout all of the integrators on clock phase 1. This also applies to the ordinary inverting integrator.

Generally, all sampled data systems that do not contain at least a single sample delay should not be cascaded because of the settling problems implicated by that construct.

3.4 Differentiators

Another very useful building block is the differentiator. It has not been used very much in filter design, but it can be very useful.

For building switched current differentiators we will make use of the core component shown in Fig. 3.12. In order to make this circuit work, the input signal has to be sampled

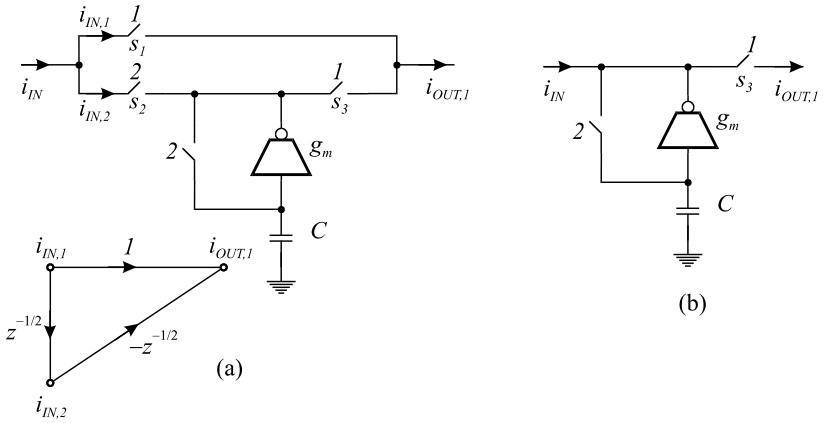

Figure 3.12: (a) Core component in all switched current differentiators; (b) Simplified Core component used in all switched current differentiators

and held for a whole clock period i.e. on both clock phase 1 and 2. In Fig. 3.12 (a) we have shown a SFG illustrating the signal flow in the core component. Using Masons formula we can now easily calculate the transfer function as being

$$H(z) = \frac{I_{out,1}}{I_{in,1}} = 1 + z^{-1/2} \cdot (-z^{-1/2}) = 1 - z^{-1} \tag{3.20}$$

If we take into account the current loss found in the CCOP we get that the transfer function of the differentiator is given by

$$H(z) = \frac{I_{out,1}}{I_{in,1}} = 1 + z^{-1/2} \cdot (-(1-\epsilon)z^{-1/2}) = (1 - z^{-1}) + \epsilon z^{-1} \tag{3.21}$$

which shows that the current loss leaks some of the input signal to the output of the integrator. The DC-gain of an ideal differentiator is zero, but the DC-gain of the leaky differentiator is

$$H(z)|_{z=1} = \epsilon \tag{3.22}$$

By investigating the circuit in Fig. 3.12 (a) we see that the switches S_1 and S_2 are logically in parallel and operating on opposite clock phases. Therefore these two switches can be replaced by a short circuit as shown in Fig. 3.12 (b).

One problem with the core circuit shown in Fig. 3.12 (b) is that it is not possible to cascade them. The reason for this is that the input signal must be valid in both clock phase 1 and 2, but the output signal is only valid on clock phase 1. To circumvent this a track and hold can be placed at the output of the core component, making the output signal valid for both clock phases. Such an arrangement is shown in Fig. 3.13 (a). The track and hold has an optional scaling factor a, giving an transfer function of

$$H(z) = -a(1 - z^{-1}) \tag{3.23}$$

Thus we have an inverting differentiator with an optional scaling a. By exchanging the differentiator and the track and hold, we arrive at the circuit shown in Fig. 3.13 (b), which

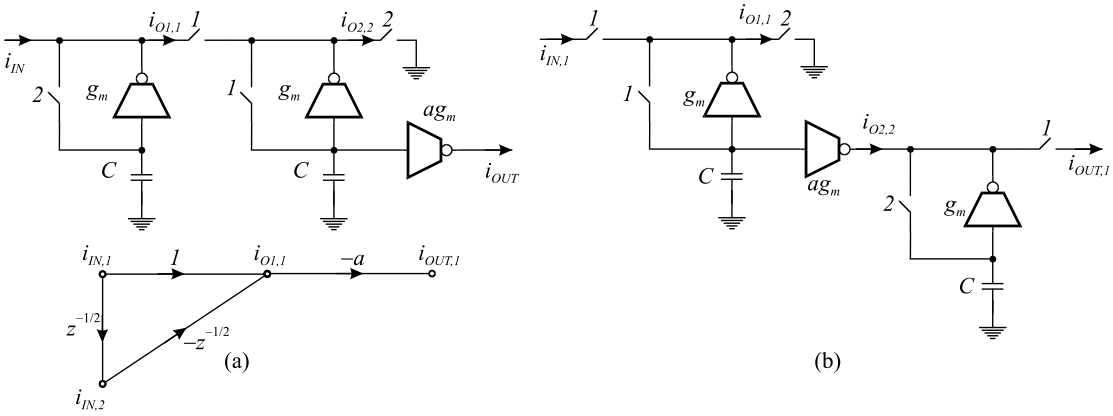

Figure 3.13: (a) Differentiator followed by a Track and Hold; (b) Track and Hold followed by a Differentiator

of course will have the same transfer function as the differentiator in Fig. 3.13 (a). The only difference is that the signal only have to be valid on clock phase 1.

The topology of the differentiator shown in Fig. 3.13 applies to all of the Cascode current copiers described in the previous chapter with the exception of the Cascode II CCOP, this is easily seen if we replace the transconductors in Fig. 3.13 by the transconductors used in Fig. 2.2 and Fig. 2.3 that have been enhanced by current conveyors.

A differentiator made from the Cascode II structure is shown in Fig. 3.14 (a). By inves-

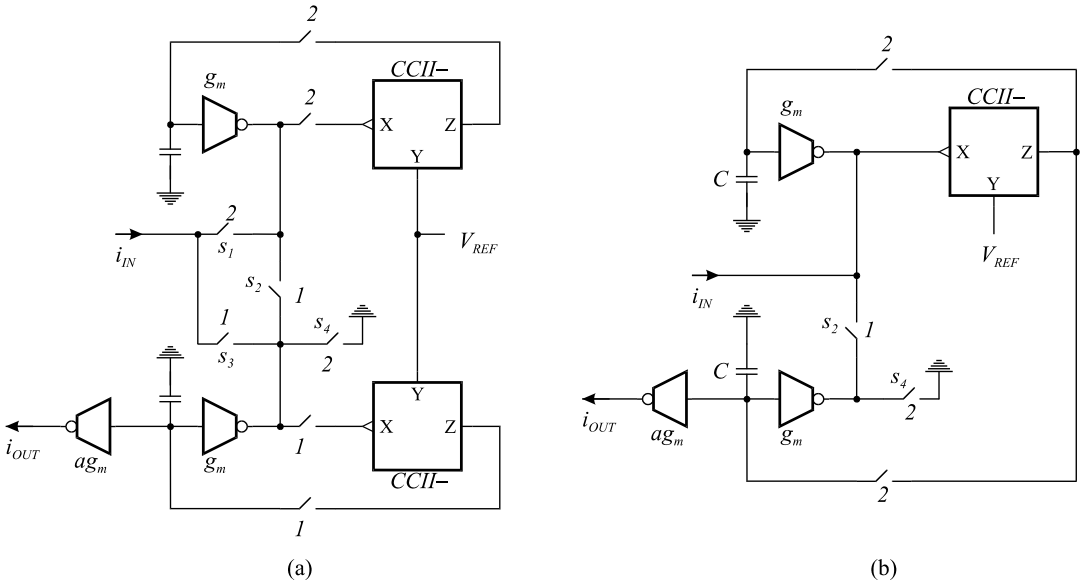

Figure 3.14: (a) Differentiator based on the Cascode II current copier; (b) Simplified differentiator

tigating this circuit we see that the switches S_1 and S_3 are logically in parallel and operating on opposite clock phases. Therefore the switch S_1 can be replaced by a short circuit and the switch S_3 removed, as shown in Fig. 3.14 (b).

To illustrate how the differentiator shown in Fig. 3.14 (b) can be implemented, we have

made two examples as shown in Fig. 3.15. In both examples the transconductors are imple-

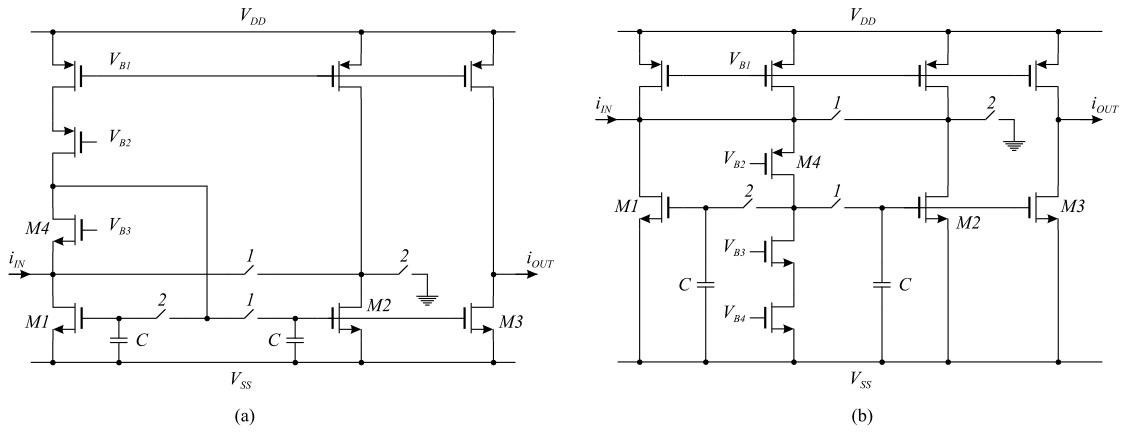

Figure 3.15: (a) Cascode implementation of differentiator; (b) Folded Cascode implementation of differentiator

mented as single NMOS transistors M1, M2 and M3. In the first example (a) the current conveyor (M4) is implemented using a NMOS transistor and in the second example (b) the current conveyor (M4) is implemented using a PMOS transistor.

The storage capacitor shown as C can be the gate-source capacitor of the transistors M1 and M2.