Chapter 4

Settling Errors in Switched Current Circuits

In this chapter we discuss how linear and *nonlinear* settling errors affect the operation of current copiers, sample delays and integrators. In this discussion we cover both single ended and fully differential SI circuits.

For medium speed, low-noise SI circuits the settling behavior will be damped and determined by the bandwidth of the current copier. In order to investigate the effect of this settling behavior on the signal processing operation of the current copier we will make use of the following figure.

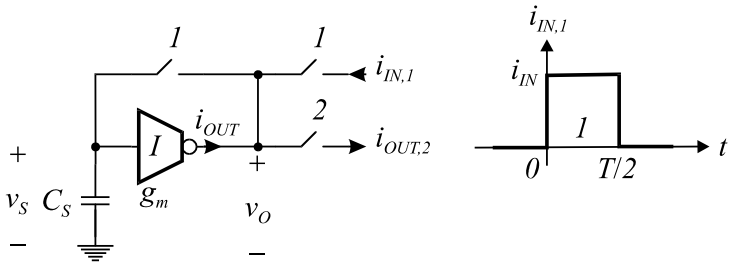

Figure 4.1: A current copier without its parasitics.

4.1 Linear Settling Errors

Assuming that we have a linear transconductor the current copier is a linear system. Therefore the transfer function of the current copier including settling errors can be found from the impulse response sequence. That is, by applying a single current pulse at the input of the current copier and observing the associated output sequence we can determine the overall transfer function of the current copier.

In the copy phase i.e. phase 1, the transfer function from the input current $i_{IN,1}$ to the voltage on the storage capacitor v_S is given by (see Appendix B and Appendix C)

$$\frac{v_S}{i_{IN,1}} = \frac{1}{g_m}\frac{\omega_o}{s+\omega_o} \tag{4.1}$$

where $\omega_0 = \frac{g_m}{C_s}$ is the bandwidth of the current copier. This is simple first order transfer function resulting in a well known exponential settling behavior.

If we assume that the initial voltage on the storage capacitor C_S is zero, a single current pulse at the input of the current copier shown in Fig. 4.1 will cause a voltage sequence at the storage capacitor as shown in Fig. 4.2.

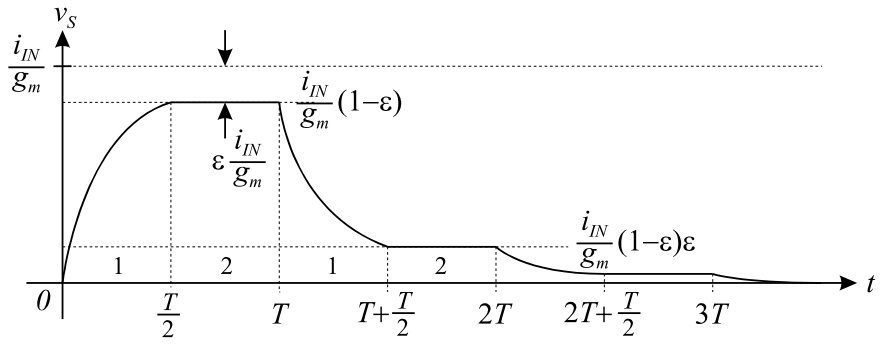

Figure 4.2: Voltage sequence at the storage capacitor in the linear current copier, for a single current pulse at the input.

The shape of this voltage sequence can be explained in the following way: In the first clock phase 1, the input signal current i_{IN} enters the current copier, resulting in an exponential charging of the storage capacitor as shown in Fig. 4.2 for $0 \leq t \leq \frac{T}{2}$.

Therefore at the end of the first clock phase 1, the voltage v_S on the storage capacitor will have charged to

$$v_S(\frac{T}{2}) = \frac{i_{IN}}{g_m}\left(1 - e^{-\omega_0 \frac{T}{2}}\right) = \frac{i_{IN}}{g_m}(1-\epsilon) \tag{4.2}$$

where

$$\underline{\epsilon = e^{-\omega_0 \frac{T}{2}}} \tag{4.3}$$

is the settling error of the current copier. This voltage is now held on the storage capacitor throughout the clock phase 2.

At the next phase 1 the input current to the current copier is now zero, effectively discharging the storage capacitor as shown in Fig. 4.2 for $T \leq t \leq T + \frac{T}{2}$.

At the end of the second clock phase 1, the voltage v_S on the storage capacitor will have charged to

$$v_S(T + \frac{T}{2}) = \frac{i_{IN}}{g_m}\left(1 - e^{-\omega_0 \frac{T}{2}}\right) e^{-\omega_0 \frac{T}{2}} = \frac{i_{IN}}{g_m}(1-\epsilon)\epsilon \tag{4.4}$$

By continuing this reasoning we get that the voltage at the storage capacitor for a single input current pulse, at the end of the n'th clock phase 1, is given by

$$v_S(nT + \frac{T}{2}) = \frac{i_{IN}}{g_m}\left(1 - e^{-\omega_0 \frac{T}{2}}\right) e^{-\omega_0 n\frac{T}{2}} = \frac{i_{IN}}{g_m}(1-\epsilon)\epsilon^n \tag{4.5}$$

From this equation we find that the output current from the current copier at the beginning of the n'th clock phase 2 is given by

$$i_{OUT,2}(nT + \frac{T}{2}) = -g_m v_S(nT + \frac{T}{2}) = -i_{IN}(1-\epsilon)\epsilon^n \tag{4.6}$$

What we are actually interested in, is the output current of the current copier at the end of the n'th clock phase 2. From the above equation we see that this current is given by

$$\underline{i_{OUT,2}(nT) = -g_m v_S(nT) = -i_{IN}(1-\epsilon)\epsilon^{n-1/2}} \tag{4.7}$$

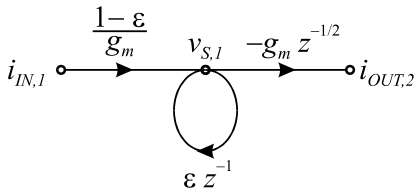

Figure 4.3: SFG describing the effect of linear settling error in a current copier.

The description of the settling behavior for a linear current copier can elegantly be summarized in a single signal flow graph, as shown in Fig. 4.3. From this SFG, and using Masons formula, we get that a current copier with a linear settling errors has a transfer function that is given by

$$\underline{H(z) = -z^{-1/2} \cdot \frac{1-\epsilon}{1-\epsilon z^{-1}}} \tag{4.8}$$

This equation shows that the transfer function of a linear current copier with settling errors, is the same as the transfer function of an ideal current copier $-z^{-1/2}$, multiplied by an error term which gives raise to a lowpass filtering operation.

The DC-gain of the linear current copier with settling errors is given by

$$H(z)|_{z=1} = -1 \tag{4.9}$$

and the gain at half the sampling frequency is given by

$$|H(z)|_{z=-1} = \frac{1-\epsilon}{1+\epsilon} \tag{4.10}$$

4.2 Nonlinear Settling Errors

In the previous section we described the settling errors in a current copier under the assumption that the transconductor was linear and had a transconductance of g_m. In most practical SI circuits the transconductor is not linear and the settling errors will become nonlinear.

In this section we will try to illustrate the effect of nonlinear settling errors on the operation of the current copier. We will assume that the transconductor used in the current copier has the following relationship between its output current and input voltage (see Fig. 4.1)

$$i_{OUT} = -If(v_S) \tag{4.11}$$

This relationship is plotted in Fig. 4.4. Based on the above assumptions and Fig. 4.1 the following differential equation can now be derived, describing the relationship between the input current i_{IN}, the voltage v_S and the output current i_{OUT}.

$$C_S \frac{\partial v_S}{\partial t} + If(v_S) = i_{IN} \tag{4.12}$$

$$i_{OUT} = -If(v_S) \tag{4.13}$$

Because the function $f(\cdot)$ could be nonlinear, the above differential equation is generally difficult to solve. But in order to be able to proceed our analysis we will assume that the nonlinearity in $f(\cdot)$ is weak and that the nonlinear transconductance can be modeled as

$$If(v_S) = g_m v_S + I\epsilon(v_S) \tag{4.14}$$

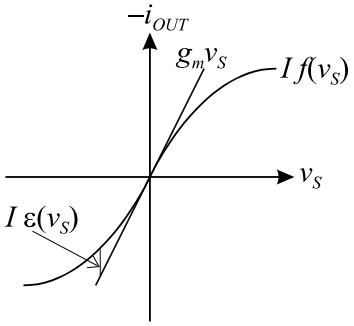

Figure 4.4: Nonlinear transconductor used in the current copier

In this equation g_m represents the linear part of $If(v_S)$ and $I\epsilon(v_S)$ represents the nonlinear part of $If(v_S)$, this is illustrated in Fig. 4.4.

If we assume that the transconductor is linear i.e. $\epsilon(v_S) = 0$, the differential equation shown in (4.12) is reduced to

$$C_S \frac{\partial v_{S0}}{\partial t} + g_m v_{S0} = i_{IN} \tag{4.15}$$

where v_{S0} is the voltage on the storage capacitor C_S for a linear transconductor.

If the nonlinearity $\epsilon(v_S)$ is small it is reasonable to assume that the voltage v_S on the storage capacitor C_S can be modeled as

$$v_S = v_{S0} + \Delta v_S \tag{4.16}$$

where v_{S0} is the voltage on the storage capacitor if there was no nonlinearity and Δv_S is the error voltage caused by the nonlinear term $\epsilon(v_S)$. If we insert (4.16) into (4.12) and combine that result with (4.15) we get that

$$C_S \frac{\partial \Delta v_S}{\partial t} + g_m \Delta v_S = -I\epsilon(v_{S0} + \Delta v_S) \tag{4.17}$$

because we previously assumed that the nonlinear term in $f(\cdot)$ was small the above equation can now be approximated by

$$C_S \frac{\partial \Delta v_S}{\partial t} + g_m \Delta v_S = -I\epsilon(v_{S0}) \tag{4.18}$$

This equation shows that the error voltage Δv_S can be found by applying a distorted version of the linear voltage v_{S0} to the input of the linear current copier. From (4.13) we get that the output current i_{OUT} is given by

$$-i_{OUT} = g_m v_{S0} + g_m \Delta v_S + I\epsilon(v_{S0}) \tag{4.19}$$

which shows that the output current from the nonlinear current copier is made from a linear term $g_m v_{S0}$ and two nonlinear terms. From the above equations it can be a bit difficult to get an idea of how the nonlinear settling errors are generated.

But if we combine (4.15), (4.18) and (4.19) into a single block diagram as shown in Fig. 4.5 we might get an idea. The block diagram shown in Fig. 4.5 can be reduced to a new block diagram as shown in Fig. 4.6.

Assuming that we have an input signal to the nonlinear current copier that is a sampled sine wave with a constant amplitude and an increasing frequency, we get from Fig. 4.6 that

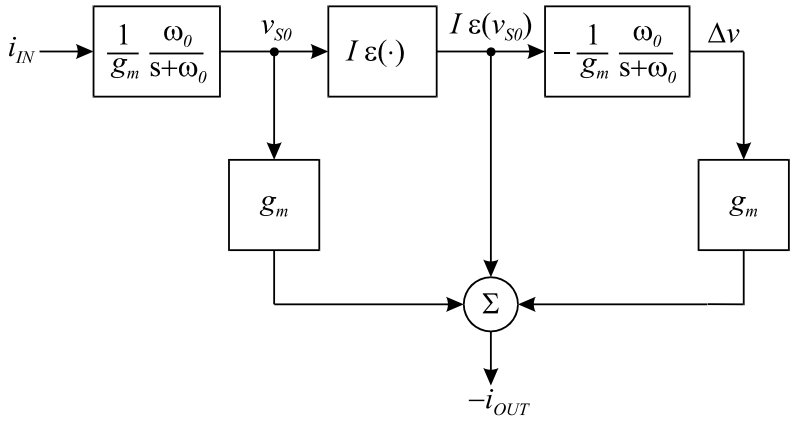

Figure 4.5: Block diagram showing the generation of the distorted output current in a nonlinear current copier

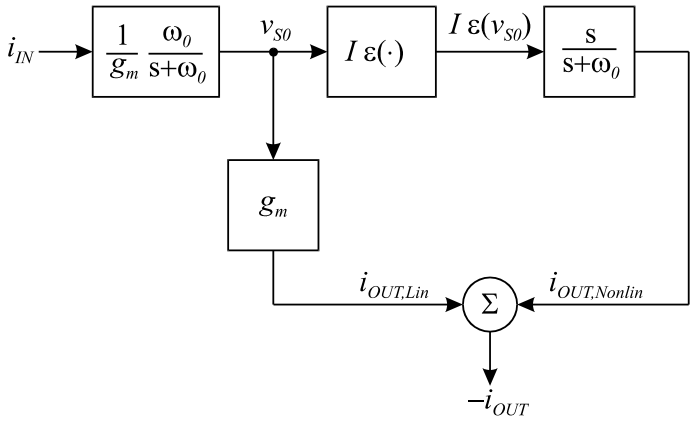

Figure 4.6: Simplified block diagram showing the generation of the distorted output current in a nonlinear current copier

the frequency content in the nonlinear current term $I\epsilon(v_{S0})$ will increase with the frequency of the input signal. The effect of this is an increased nonlinear signal $i_{OUT,Nonlin}$ because of the highpass filtering, which in turn increases the distortion at the output of the current copier.

The conclusion is therefore, that for an input signal with a constant input amplitude the distortion at the output of a current copier, caused by nonlinear settling errors, will increases with the frequency of the input signal. And because of the sampling the distortion will be symmetrical around half the sampling frequency.

It is difficult to derive an analytical expression for the actual distortion as a function of the amplitude of the input signal, the transconductor nonlinearity and the signal frequency.

Some attempts have been made for estimating the worst case distortion at the output of a current copier [28]. But the results found in [28] are of little use for practical applications because the estimated worstcase distortion, could deviate by a factor of five from the actual value.

In practical situations the only way to get accurate distortion results, is by simulating the switch current circuit using the actual nonlinearities and component values.

At the moment there exist several simulators for simulating analog sampled data systems, but unfortunately they all assume that the circuits are linear, so we dont get any distortion results. The only simulator at the moment that is capable of simulating nonlinearities in switched current circuits, is SPICE.

If we e.g.want to simulate the distortion at the output of a switched current Sigma-Delta modulator it is practically impossible to use SPICE for that job, because the simulation time might be weeks or even months, in order to get enough samples out of the modulator.

In order to simulate nonlinearities in large switch current circuits I found that it was necessary to have a simulator capable of performing both linear behavior modeling and a more detailed nonlinear simulations. For this job, I have written a small simulator package in C++ that I have used to illustrate the distortion mechanisms caused by nonlinear settling errors.

Example 4.2.1
The following example will illustrate how nonlinear settling errors influence the distortion in switched current circuits. The example will cover current copiers, sample delays and integrators. The simulations in this example are all performed using my own switched current simulator package,

The current copier used in the following examples is the same as the one used in [28]. The diagram of the current copier cell is shown in Fig. 4.7 and the parameters are listed in Table 4.1

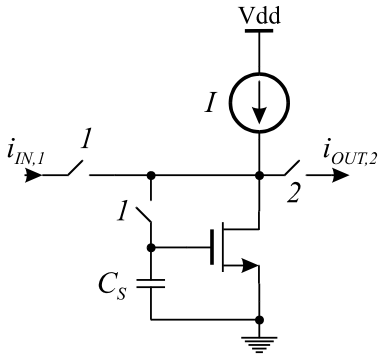

Figure 4.7: Current copier used for distortion simulations

Table 4.1: Parameters used for the current copier

Parameter		*Value*
Sampling frequency	f_s	$512kHz$
Storage capacitance	C_S	$22.08pF$
Small-signal transconductance	g_m	$85.16\mu A/v$
Quiescent current	I	$20\mu A$
Modulation index	m	0.5

Based on the results in Table 4.1 we are able to calculated the following parameters:

Saturation voltage:	$\Delta v = \frac{2I}{g_m} = 0.47V$
Small-signal bandwidth:	$\omega_0 = \frac{g_m}{C_S} = 3.857\text{MhZ}$
Small-signal settling error:	$\epsilon = e^{-\omega_0 \frac{T}{2}} = e^{-3.867 \cdot 10^6 \cdot 977nS} = 2.27\%$

We notice that the small-signal settling error is rather large: 2.27%. Therefore we might expect a lot of distortion from the current copier.

4.2.1 Current Copier

A distortion simulation was performed by applying a 16kHz sine wave as input to the current copier shown in Fig. 4.7, and with the parameters shown in Table 4.1. The simulation was performed using a switched current simulator written in C++. On each clock phase, the C++ simulator solves the nonlinear differential equation (4.12), using 2nd order Runge Kutta algorithm.

The reason for using a dedicated simulator written in C++, is that it is much faster than SPICE, because it only considers effects that are important for the distortion simulation, whereas SPICE spends a lot of time calculating small glitches that occur everytime the switches are clocked.

In Fig. 4.8, we have shown the frequency spectrum at the output of the current copier. The frequency spectrum was found by taking the FFT of the windowed simulation sequence. The window function used in this example is a Kaiser-Bessel window. For comparison with

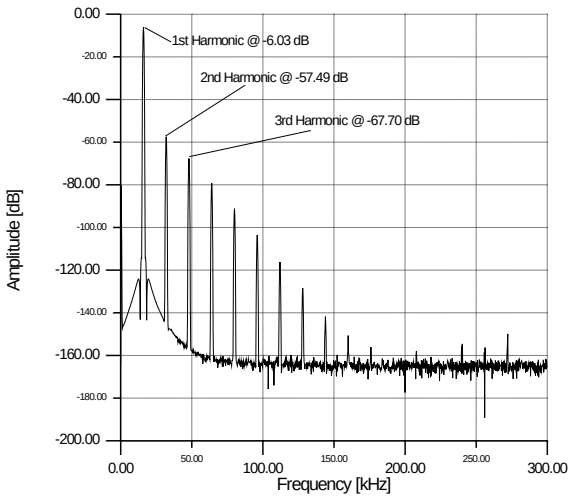

Figure 4.8: Frequency spectrum at the output of the current copier

[28] we se from our simulation in Fig. 4.8 that the first three harmonics are at the levels $\{-6.03\text{dB}, -57.49\text{db}, -67.70\text{dB}\}$ whereas in [28] they are located at $\{-6.0009\text{dB}, -60.72\text{db}, -67.41\text{dB}\}$. This indicates that the C++ simulator gives results that are consistent with the results found using HSPICE simulations in [28].

We notice that there is a lot of distortion at the output of the current copier, consisting of both even and odd order harmonics. The even order harmonics are caused by the asymmetrical output signal, which is due to the asymmetrical nonlinearity (square law) of the transconductor used in the current copier (MOS transistor).

If we had implemented the current copier using a symmetrical nonlinearity (e.g. a MOS Differential pair) there would not have been any even order harmonics in the output spectrum.

The distortion at the output of the current copier for various input frequencies is shown in Fig. 4.9. This figure shows that the distortion increases approximately by 20dB/dec. with

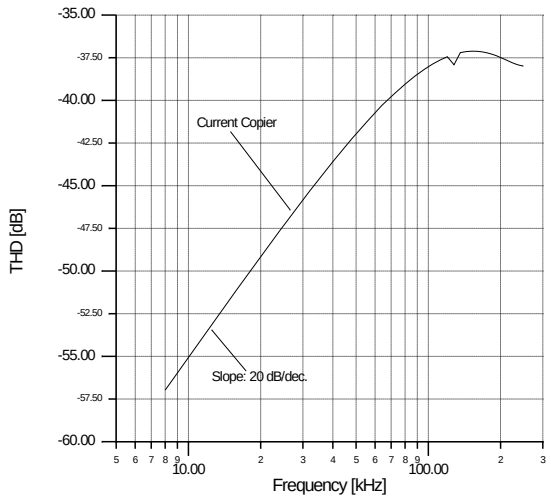

Figure 4.9: Distortion (THD) as a function of input frequency for the current copier

the frequency of the input signal. This can be explained in the following way: when we increase the frequency of the input signal by a decade (factor of 10), the frequency content of the error signal, $I\epsilon(v_o)$ in Fig. 4.6, also increases by the same amount. Therefore the derivative (highpass filtering) of this error signal, $i_{OUT,Nonlin}$, will also increase by a factor of 10, leading to the increased distortion of 20dB/dec. This relationship between distortion and input signal frequency was also observed in [28].

From these observations we can now conclude that it might be advantageous to use oversampling of the signals as a technique for reducing the distortion caused by nonlinear settling. There is however a lower bound on the available distortion which is determined by i.e. clock feedthrough and charge injection from the switches [28].

4.2.2 Sample Delays

The same distortion measurement, as used on the current copier is now performed on a sample delay i.e. a cascade connection of two current copiers.

In Fig. 4.10 we have the frequency spectrum at the output of the sample delay. If we compare Fig. 4.8 and Fig. 4.10 we notice that the 2nd order harmonic in Fig. 4.8 has been reduced by $60.81dB$ and that the 3rd harmonic in Fig. 4.8 has been increased by $6.01dB$.

This can be explained in the following way: The output signal of the first current copier is an inverted and distorted version of the input signal (see Fig. 4.8). This signal is now applied to the input of the next current copier, leading to an almost symmetrical output signal from the second current copier. This means that the output spectrum of the sample delay has almost no even order harmonics but the odd harmonics will have twice the amplitude of a single current copier.

By connecting two sample delays in series i.e. a series connection of four current copiers we get the frequency spectrum shown in Fig. 4.11 If we compare Fig. 4.10 and Fig. 4.11 we notice that the spectra are almost identical, the only difference is that the 2nd harmonic

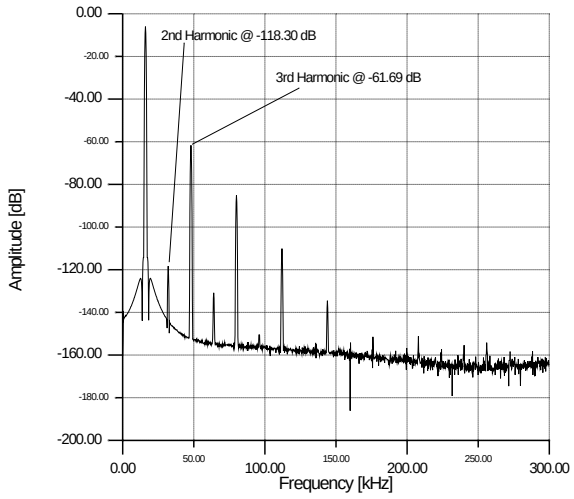

Figure 4.10: Frequency spectrum at the output of the sample delay

in Fig. 4.10 has been increased by 5.84dB and that the 3rd harmonic in Fig. 4.10 has been increased by 5.95dB.

This can be explained in the following way: The output signal of the first sample delay is a distorted version of the input signal, dominated by odd harmonics Fig. 4.10. This signal is now applied to the input of the next sample delay, similar to the first one, which operates as an almost asymmetrical nonlinearity leading to an increased distortion of 6dB.

The distortion at the output of the current copier and the sample delays for various input frequencies is shown in Fig. 4.12. This figure shows that the distortion increases approximately by 20dB/dec. with the frequency of the input signal. From Fig. 4.12 we notice that a single current copier generates almost as much distortion as a series connection of four current copiers. This result only applies for current copiers made from asymmetrical transconductor e.g. single MOS transistor. We also notice that for each sample delay i.e. a pair of current copiers, the distortion increases by a factor of two (6dB). This applies for all switched current circuits.

4.2.3 Integrators

In order to illustrate the distortion behavior in switched current integrators, a simulation setup has been made, where the output of the sample delay is connected back to its input, resulting in a integrator (see Chapter 3).

The input signal to the integrator is a sine wave with a frequency of 16kHz and, in order to be able to compare the simulations result found for the integrator with those found for the current copier and the sample delays, *the amplitude of the input signal to the integrator has been adjusted with frequency, so that the amplitude of the output signals from the integrator is independent of the frequency and has the same magnitude, as the output signals of the current copier and the sample delays.*

There are basically two current outputs from a switched current integrator: inverting and noninverting, that can be found as the output of the first and the second current copier respectively.

The distortion at the inverting and the noninverting outputs is shown in Fig. 4.13 and

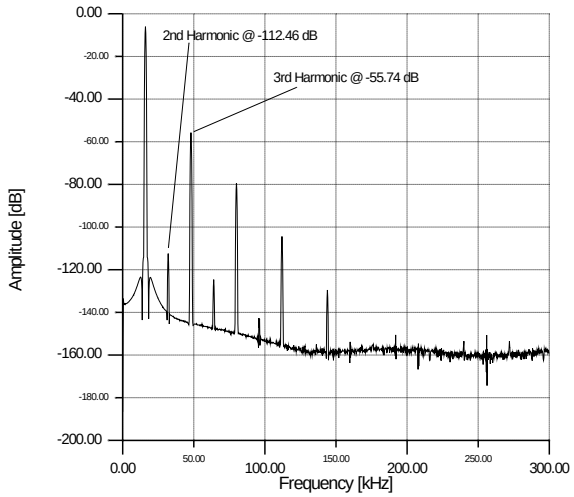

Figure 4.11: Frequency spectrum at the output of the double sample delay

Fig. 4.14. From Fig. 4.13 we notice that the distortion at the inverting output is very similar to the distortion found at the output of a single current copier Fig. 4.8. Even the amplitude of the harmonics is almost the same with the exception that the 3rd harmonic in Fig. 4.13 is a little bit higher that the 3rd harmonic in Fig. 4.8.

From Fig. 4.14 we notice that the distortion at the noninverting output is very similar to the distortion found at the output of a sample delay Fig. 4.10. The amplitude of the even harmonics in Fig. 4.14 are though somewhat higher than the even harmonics at the output of the sample delay Fig. 4.10.

The distortion at the outputs of the integrator for various input frequencies is shown in Fig. 4.15. From Fig. 4.15 we se that the distortion at the noninverting output is lower than the distortion at the inverting output. Also, we notice that the interesting fact, that the distortion at the noninverting output is almost independent of the frequency. This applies only to switched current integrators built from current copiers based on asymmetrical transconductors e.g. single MOS transistors. There is however a sudden increase in the distortion at a frequency little bit lower than half the sampling frequency, the reason for this has not been discovered yet.

Symmetrical Transconductor (MOS Differential Pair)

I have also made a simulation of an integrator build from fully differential current copiers, instead of the single transistor current copier shown in Fig. 4.4. Each of the transistors in the differential pair has the same saturation voltage as the CCOP in Fig. 4.4, in order to get the same voltage signal swing, but only half the bias current $I/2$ which of course implies that the small signal transconductance is also the half. In order to maintain the same settling behavior each of the gate-source capacitors C_S have been reduced by a factor of two.

The distortion at the inverting and the noninverting outputs is shown in Fig. 4.16 and Fig. 4.17. From Fig. 4.16 and Fig. 4.17 we see that the distortion at the inverting and the noninverting outputs is similar. The harmonicas at the noninverting output are however 6dB higher that the harmonics at the inverting output.

The distortion at the outputs of the integrator for various input frequencies is shown in Fig. 4.18. From Fig. 4.18 we se that the distortion at the inverting and noninverting outputs

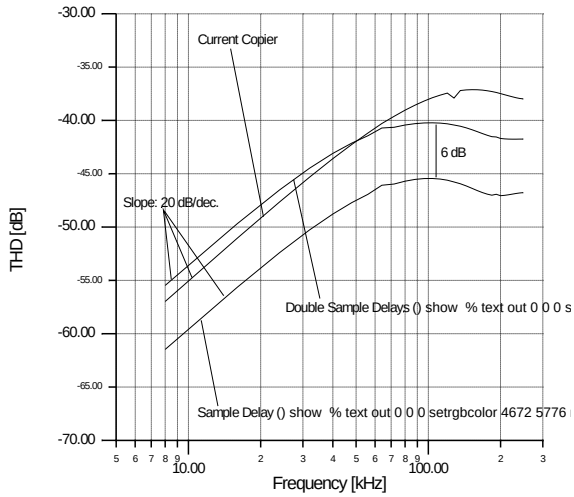

Figure 4.12: Distortion (THD) as a function of input frequency for the current copier and the sample delays

has the same dependence on the input frequency. The distortion at the noninverting output is however 6dB higher than the distortion at the inverting output. ■

4.3 Reduction of Settling errors

The nonlinear settling errors are caused by the nonlinear transconductors used in the current copiers. We have previously shown that the relationship between the input and the output current of a nonlinear current copier is given by

$$C_S \frac{\partial v_S}{\partial t} + If(v_S) = i_{IN} \tag{4.20}$$

$$i_{OUT} = -If(v_S) \tag{4.21}$$

where $If(v_S)$ represents the nonlinear transconductance, and I is the bias current. If we normalize this equation with respect to I, we get that the normalized nonlinear current copier can be described by

$$\frac{C_S}{I}\frac{\partial v_S}{\partial t} + f(v_S) = \frac{i_{IN}}{I} \tag{4.22}$$

$$\frac{i_{OUT}}{I} = -f(v_S) \tag{4.23}$$

in this equation, the modulation index of the current copier is given by $m = i_{IN}/I$ and the term C_S/I is inversely proportional to the small signal bandwidth ω_0 of the current copier.

From the above equation we see that there are basically two ways of reducing the nonlinear settling error found in switched current circuits.

1. Reduce the modulation index m i.e. reduce the signal current i_{IN} compared to the bias current I.

2. Increase the small signal bandwidth ω_0 of the current copier, by increasing the supply current I compared to the storage capacitance C.

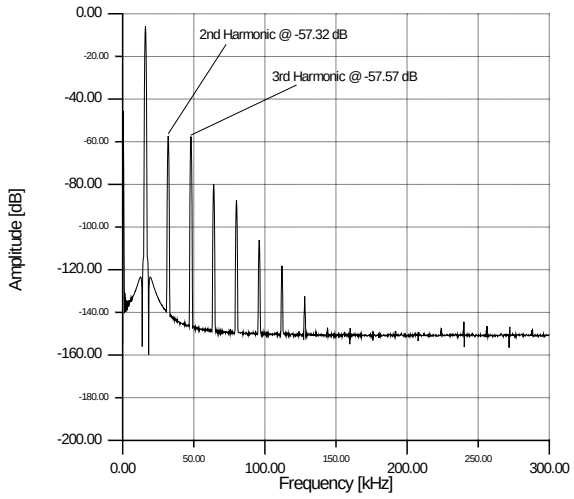

Figure 4.13: Frequency spectrum of the inverting output of the integrator

An interesting question that now arises is; which one of the two above methods should we chose for reducing the settling errors. In order to answer this question we will make a small example.

Example 4.3.1
In this example we will look at the distortion at the output of a single current copier as described previously. The example is based on the parameters shown in Table 4.1. In Fig. 4.9 we have shown that the distortion at the output of the current copier, with a modulation index $m = 0.5$ and a bias current $I = 20\mu A$, is THD $= -51.04$dB.

In order to reduce the distortion below -65dB we can either make the modulation index m somewhat smaller that 0.5, or we can make the bias current I somewhat larger than $20\mu A$.

Reduction of the modulation index m: A simulation shows that in order to reduce the distortion below -65dB, the modulation index must be lowered to $m = 0.125$ i.e. it must be made four times smaller.

Increase of the bias current I: A simulation shows that in order to reduce the distortion below -65dB, the bias current must be increased to $I = 32.5\mu A$ i.e. it must be made 1.625 times larger.

If we reduce the modulation index, we actually decrease the SNR of the current copier (see Chapter 5). By reducing the modulation index by a factor four, the SNR is reduced by 12dB, in order to compensate for this loss, we have to increase the storage capacitance C_S by factor $4^2 = 16$. Now that the storage capacitance had to be increased in order to keep up the SNR, we also have to increase the bias current I by a factor 16 in order to maintain the settling properties. By decreasing the modulation index m from 0.5 to 0.125, we have actually increased the power consumption by a factor 16.

If we instead had maintained the modulation index m at 0.5, and then increased the bias current I by a factor of 1.625 we would get the same distortion and SNR.

The conclusion is therefore, that in terms of power consumption and area, the best way to reduce the nonlinear settling errors, is to maintain the modulation index m and increase the small signal bandwidth ω_0 of the current copier, by increasing the supply current I compared to the storage capacitance C_S. ■

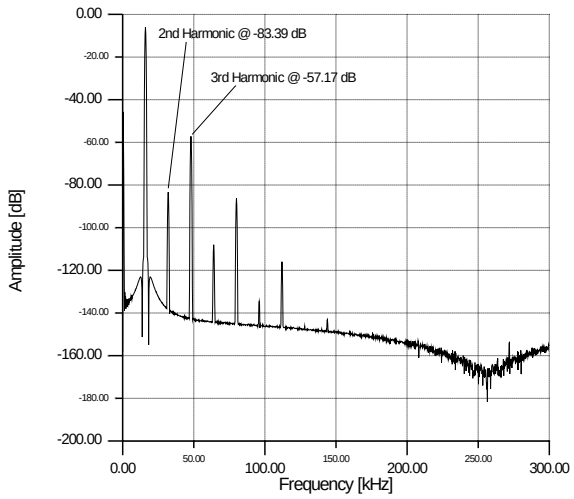

Figure 4.14: Frequency spectrum of the noninverting output of the integrator

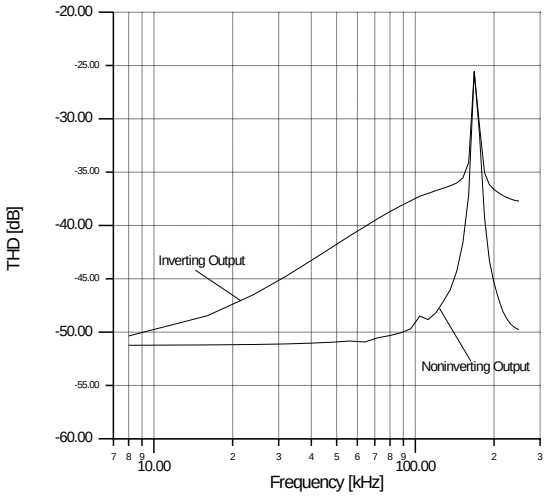

Figure 4.15: Distortion (THD) as a function of the input frequency for the integrator

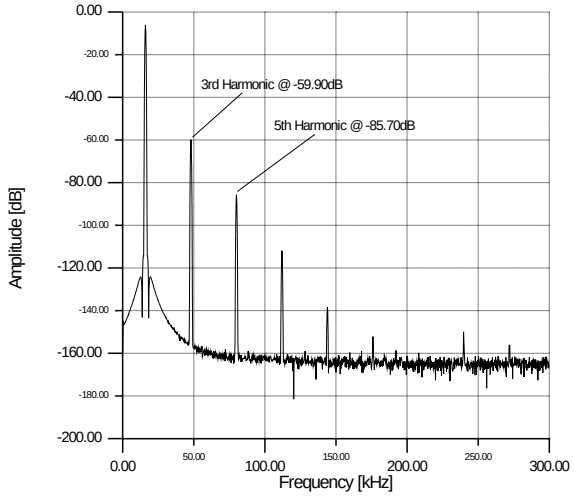

Figure 4.16: Frequency spectrum at the inverting output of the integrator (Differential Transconductor)

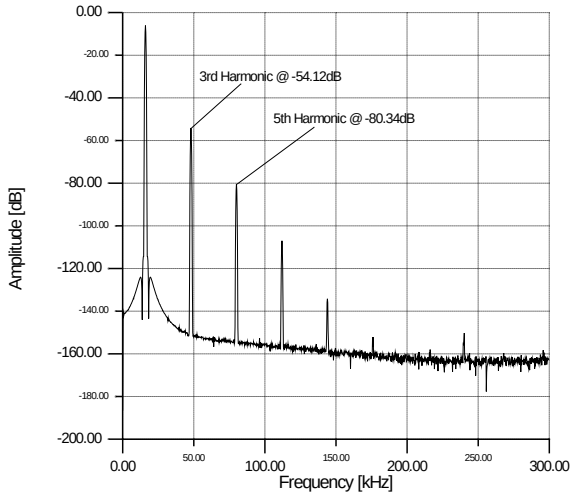

Figure 4.17: Frequency spectrum at the noninverting output of the integrator (Differential Transconductor)

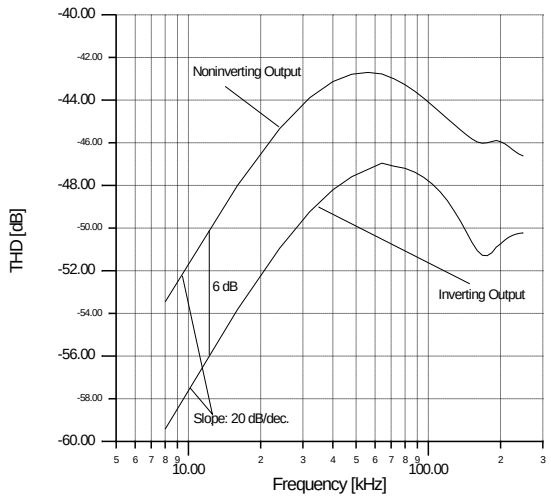

Figure 4.18: Distortion (THD) as a function of input frequency for the integrator (Differential Transconductor)