Chapter 5

Optimization of Switched Current Circuits

This chapter introduces noise analysis of SI circuits, which is one of the fundamentals for the design of high performance SI circuits. The contents of this chapter depends strongly on the results regarding sampling of noise described in Appendix E.

One of the most important results of this chapter is the connection between power consumption, supply voltage, signal to noise ratio and operating frequency. This will found the basis for optimization of SI circuits.

5.1 Introduction to Noise Analysis

Before we can perform any noise analysis of switched current circuits we have to identify all of the noise sources that are important for the analysis. In Fig. 5.1 we have shown a cascode current copier including all of its noise sources. For each MOS transistor in the circuit there is

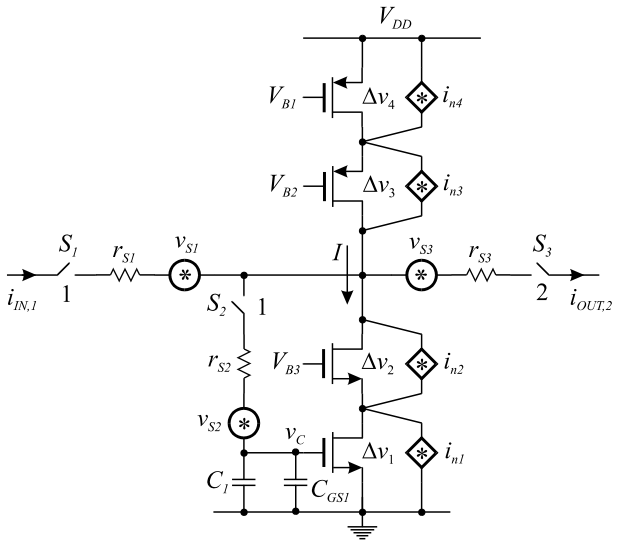

Figure 5.1: Cascode Current Copier with all Noise Sources

a corresponding current noise $i_{n1} \ldots i_{n4}$. These current noise sources could equally well have been transformed to the gate of the respective MOS transistors as a voltage noise source, by

dividing the current noise source by the square of the transconductance g_m^2. I have chosen to use current noise sources.

Each current noise source consists of both a thermal white noise source and a low frequency $1/f$ noise source, i.e. each noise source can be written as

$$i_n = i_n^w + i_n^{1/f} \tag{5.1}$$

where i_n^w represents the white noise and $i_n^{1/f}$ represents the $1/f$ noise.

We will assume that all of the transistors are operating in strong-inversion and saturation and that the white noise and the $1/f$ noise are uncorrelated. This implies that the power spectral density of the current noise can be written as

$$S_n(f) = S_n^w(f) + S_n^{1/f}(f) \tag{5.2}$$

where

$$S_n^w(f) = \frac{2}{3} 2kTg_m \tag{5.3}$$

$$S_n^{1/f}(f) = \frac{\mathrm{KF} \cdot I}{2C'_{OX}L^2|f|} \tag{5.4}$$

In the above equations $k = 1.38 \cdot 10^{-23} J/K$ represents Boltzmanns constant, T is the temperature in Kelvin, C'_{OX} is the oxide capacitance per area, L is the channel length, I is the drain current and KF is the flicker noise coefficient. In Fig. 5.1 we have also shown the voltage noise sources $v_{S1} \ldots v_{S3}$ originating from the switches $S_1 \ldots S_3$. Each of these voltage noise sources is a consequence of the on-resistance of the switches. The power spectral density of these noise sources is given by

$$S_S(f) = 2kTr_s \tag{5.5}$$

In order to make the noise analysis feasible we have to identify the noise sources that can be regarded as being small compared to the dominating noise sources. To do so we will look at the current copier in its copy phase i.e. phase 1.

We notice that all of the voltage noise sources $v_{S1} \ldots v_{S3}$ are somehow in series with the signal current source $i_{IN,1}$. This means that any voltage variations caused by these noise sources are suppressd. Therefore the noise originating from the switches can be ignored [13].

The only noise sources left are the transistors used to build the transconductor used in the current copier. The current noise originating from the cascode transistors M2 and M3 can be ignored compared to the noise originating from the memory transistor M1 and the current source M4.

In order to illustrate that the cascoding transistors will have a very little effect on the overall noise from the current copier, we will make use of Fig. 5.2. From this figure we see that the output current noise i_{no} is given by

$$i_{no} = i_{n1}\frac{g_{m2}}{g_{m2}+g_{o1}+g_{o2}} + i_{n2}\left(1 - \frac{g_{m2}}{g_{m2}+g_{o1}+g_{o2}}\right) \tag{5.6}$$

$$= i_{n1}\frac{g_{m2}}{g_{m2}+g_{o1}+g_{o2}} + i_{n2}\frac{g_{o1}+g_{o2}}{g_{m2}+g_{o1}+g_{o2}} \tag{5.7}$$

$$\simeq i_{n1} \tag{5.8}$$

This equation shows that the noise i_{n2} from the cascode transistor is approximately reduced by the intrinsic gain of the cascode transistor g_{m2}/g_{o2} compared to the noise i_{n1} from the main transistor, therefore we will ignore the noise originating from the cascode transistors.

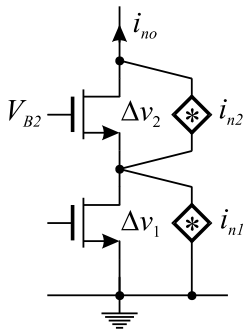

Figure 5.2: Noise from a Cascoded MOS Transistor

At this point we have seen that the dominating noise sources, in the cascodet current copier shown in Fig. 5.1, are the memory transistor M1 and the current source M4. In order to calculate the noise power at the output of the current copier, we will make use of Fig. 5.3 In Fig. 5.3 we have shown the cascode current copier with its equivalent input noise current

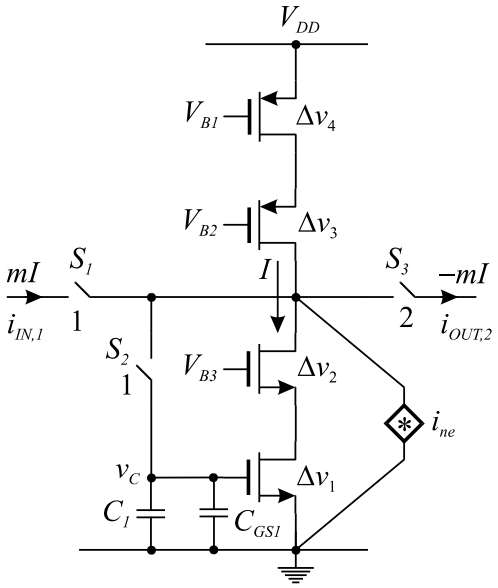

Figure 5.3: Cascode Current Copier shown with its equivalent input noise source

source i_{ne}. Based on the above conclusion and Fig. 5.1 we have that the equivalent input current noise is given by

$$i_{ne} = i_{n1} + i_{n4} \tag{5.9}$$

where i_{n1} and i_{n4} are the noise from the memory transistor and the current source.

When the current copier in Fig. 5.3 is operating, the noise source i_{ne} is sampled on clock phase 1 and 2. This sampling will affect the white noise and the $1/f$ noise part in different ways. This is best illustrated by the signal flow graph in Fig. 5.4.

This SFG shows the transfer function $-z^{-1/2}$ of the current copier between the input $i_{IN,1}$ and the output $i_{OUT,2}$. In the SFG we have also shown how the white noise part and

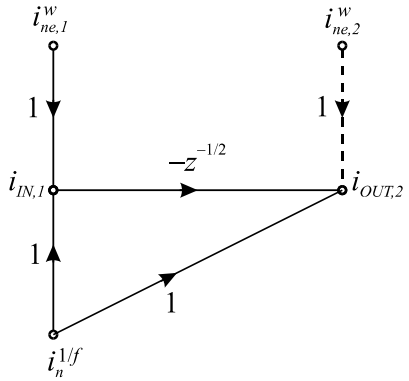

Figure 5.4: SFG representing the noise sampling

the $1/f$ noise part of the equivalent input noise i_{ne} are processed differently by the sampling process.

The noise samples taken from the white noise source at different time instances are uncorrelated, which is shown in the SFG as two independent noise sources $i^w_{ne,1}$ and $i^w_{ne,2}$. The samples taken from the white noise source on clock phase 1 are feed to the input of the current copier whereas the samples taken on clock phase 2 are feed to the output of the current copier.

In contrast to the white noise, samples taken from the $1/f$ noise are correlated which is shown in the SFG as a single $1/f$ noise source $i^{1/f}_{ne}$ feeding both the input and the output of the current copier.

From the SFG in Fig. 5.4 we have the following transferfunctions for the white noise and the $1/f$ noise

$$H^w(z) = -z^{-1/2} \tag{5.10}$$

$$H^{1/f}(z) = 1 - z^{-1/2} \tag{5.11}$$

which shows that the $1/f$ noise is exposed to correlated double sampling (CDS).

From Fig. 5.3 we see that the white noise sampled on clock phase 1 is bandlimited by the current copier itself. We will here assume that the current copier can be viewed as a first order system with a bandwidth given by

$$\omega_0 = \frac{g_{m1}}{C} \tag{5.12}$$

where C is the effective storage capacitance which is given by

$$C = C_1 + C_{GS1} \tag{5.13}$$

Based on the results found in Appendix E we find that the power spectrum for the sampled white- and $1/f$ noise is given by

$$s^w(f) = \frac{2}{3} 2kT(g_{m1} + g_{m4}) \frac{g_{m1}}{2C} \tag{5.14}$$

$$s^{1/f}(f) = f_s \left(\frac{\mathrm{KF}_N \cdot I}{2C_{OX} L_1^2 |f|} + \frac{\mathrm{KF}_P \cdot I}{2C_{OX} L_4^2 |f|} \right) \tag{5.15}$$

The noise power, at the output of the current copier, in the frequency band $[-f_S/2; +f_S/2]$ can now be found by integrating the product of the power spectrum and the squared transfer

function from the noise source to the output of the current copier. By using the results found in Appendix E, we get that the noise power at the output of the current copier is given by

$$P_n^w = \frac{2}{3}\frac{kT}{C}g_{m1}^2\left(1+\frac{g_{m4}}{g_{m1}}\right) \tag{5.16}$$

$$P_n^{1/f} = 2.2272\frac{\mathrm{KF}_N \cdot I}{2C_{OX}L_1^2}\left(1+\frac{\mathrm{KF}_P}{\mathrm{KF}_N}\left(\frac{L_1}{L_4}\right)^2\right) \tag{5.17}$$

Because the transfer function of the current copier is an inverting half clock sample delay, the amplitude of the output signal is the same as the amplitude of the input signal. The input signal current to the current copier is a fraction m ($|m| \leq 1$) of the bias current I. This fraction is called the modulation index of the current copier. Based on this, the power of the signal current at the output of the current copier (assuming that it is a sine wave) is given by

$$P_s = \frac{m^2 I^2}{2} \tag{5.18}$$

We will now define the signal-to-noise-ratio (SNR) as being the ratio between the signal power and the noise power i.e.

$$SNR = \frac{P_s}{P_n^w + P_n^{1/f}} \tag{5.19}$$

$$= \frac{P_s}{P_n^w}\cdot\frac{1}{1+\frac{P_n^{1/f}}{P_n^w}} \tag{5.20}$$

An interesting factor in this equation, is the ratio between the power of the $1/f$ noise and the white noise. This ratio is given by

$$\frac{P_n^{1/f}}{P_n^w} = \frac{2.2272\frac{\mathrm{KF}_N \cdot I}{2C_{OX}L_1^2}\left(1+\frac{\mathrm{KF}_P}{\mathrm{KF}_N}\left(\frac{L_1}{L_4}\right)^2\right)}{\frac{2}{3}\frac{kT}{C}g_{m1}^2\left(1+\frac{g_{m4}}{g_{m1}}\right)} \tag{5.21}$$

$$= \frac{C}{\frac{2}{3}C_{OX}W_1L_1}\cdot\frac{2.2272\cdot\mathrm{KF}_N}{2kT\cdot K_N'}\cdot\frac{1+\frac{\mathrm{KF}_P}{\mathrm{KF}_N}\left(\frac{L_1}{L_4}\right)^2}{1+\frac{\Delta v_1}{\Delta v_4}} \tag{5.22}$$

Example 5.1.1
For a typical $2.4\mu m$ CMOS process (MIETEC) we have the following parameters

$$\mathrm{KF}_N = 2.3\cdot 10^{-27} \tag{5.23}$$

$$\mathrm{KF}_P = 7.2\cdot 10^{-29} \tag{5.24}$$

$$K_N' = 57\mu A/V^2 \tag{5.25}$$

$$K_P' = 17\mu A/V^2 \tag{5.26}$$

Using these parameters at a temperature of $T = 300K$, we get that the ratio between the power of the $1/f$ noise and the white noise is given by

$$\frac{P_n^{1/f}}{P_n^w} = \frac{C}{C_{GS1}}\cdot 0.01085\cdot\frac{1+0.0313\left(\frac{L_1}{L_4}\right)^2}{1+\frac{\Delta v_1}{\Delta v_4}} \tag{5.27}$$

If we assume that the memory transistor and the current source have the same channel lengths and the same saturation voltages, we get that

$$\frac{P_n^{1/f}}{P_n^w} = \frac{C}{C_{GS1}} \cdot 0.0056 = \left(1 + \frac{C_1}{C_{GS1}}\right) \cdot 0.0056 \tag{5.28}$$

from this equation we see that as long as the external storage capacitance C_1 is less than 178 times the gate-source capacitance C_{GS1} of the memory transistor, the white noise will be larger than the $1/f$ noise. Often the external storage capacitance C_1 is equal to zero making the effective storage capacitance equal to the gate-source capacitance C_{GS1}. In these cases the noise power is dominated by the white noise, and the $1/f$ noise can be neglected if it is exposed to CDS. ■

From the above example we can therefore conclude that if the $1/f$ noise is exposed to CDS, the SNR is closely approximated by the ratio between the signal power and the noise power of the white noise.

$$\underline{SNR \simeq \frac{P_s}{P_n^w}} \tag{5.29}$$

5.1.1 Signal to Noise Ratio SNR

If we insert (5.16) and (5.18) into (5.29) we get that the SNR is given by

$$SNR \simeq \frac{\frac{m^2 I^2}{2}}{\frac{2}{3}\frac{kT}{C} g_{m1}^2 \left(1 + \frac{g_{m4}}{g_{m1}}\right)} \tag{5.30}$$

$$= \frac{m^2 \cdot I^2}{\frac{4}{3}\frac{kT}{C} g_{m1}^2 \left(1 + \frac{g_{m4}}{g_{m1}}\right)} \tag{5.31}$$

$$= C \cdot \frac{m^2 \cdot \Delta v_1^2}{\frac{16}{3} kT \left(1 + \frac{\Delta v_1}{\Delta v_4}\right)} \tag{5.32}$$

It is interesting to note that the above equation states that the SNR depends only on the storage capacitance C, the modulation index m and on the saturation voltages $\{\Delta v_1, \Delta v_4\}$ chosen for the transistors. The SNR does not depend on the choice of the bias current I, which is bounded by some other constraints i.e. the operating speed and the settling errors (see Chapter 4).

We notice that the SNR can be increased by increasing the storage capacitor or by increasing the saturation voltages $\{\Delta v_1, \Delta v_4\}$. This shows that there is a trade off between the size of the storage capacitance and the minimum supply voltage. We might therefore expect that low-noise circuits with reasonable capacitor sizes are not suitable for low voltage operation.

5.1.2 Storage Capacitance

By rearranging the expression for the SNR we get that the storage capacitance is given by

$$C = SNR \cdot \frac{16}{3} kT \frac{\left(1 + \frac{\Delta v_1}{\Delta v_4}\right)}{m^2 \cdot \Delta v_1^2} \tag{5.33}$$

An important observation from the above equation is that if we increase the SNR by 6dB i.e. 1−Bit, we have to increase the storage capacitor by a factor of four !. Remember that the SNR is defined as a power ratio.

Also we notice that in order to minimize the storage capacitance for a given SNR, we have to make the saturation voltages $\{\Delta v_1, \Delta v_4\}$ as large as possible i.e. we have to have a large supply voltage.

5.1.3 Bias Current

The bandwidth of the current copier is determined by the storage capacitance C and the small signal transconductance g_{m1} of the memory transistor, we have that

$$\omega_o = \frac{g_{m1}}{C} = \frac{2I}{\Delta v_1 C} \tag{5.34}$$

which gives the following relationship for the bias current I.

$$I = \omega_o C \frac{\Delta v_1}{2} \tag{5.35}$$

By combining this equation with the expression for the storage capacitance we get that the bias current is given by

$$I = \omega_o \cdot SNR \cdot \frac{16}{3} kT \frac{\left(1 + \frac{\Delta v_1}{\Delta v_4}\right)}{m^2 \cdot \Delta v_1} \tag{5.36}$$

This equation shows that for a given operating speed ω_0 and a given signal-to-noise-ratio SNR, the only way to reduce the current consumption is to increase the saturation voltages $\{\Delta v_1, \Delta v_4\}$ i.e. we have to increase the supply voltage.

This indicates that for some SI circuits the power consumption might be almost independent of the supply voltage.

5.1.4 Power Consumption

The current copier is operating in class A, which implies that the power consumption is found as the product of bias current and supply voltage, we have

$$P_{sup} = V_{DD} \cdot I = V_{DD} \cdot \omega_o \cdot SNR \cdot \frac{16}{3} kT \frac{\left(1 + \frac{\Delta v_1}{\Delta v_4}\right)}{m^2 \cdot \Delta v_1} \tag{5.37}$$

This equation shows us that the power consumption of SI circuits increases if we increase the operating speed or the signal-to-noise-ratio SNR.

5.1.5 Constraints

Once we have chosen a specific circuit topology for our SI circuit it becomes evident that there exist some constraints that have to be fulfilled so that our circuit can operate properly.

These constraints give a relationship between the supply voltage V_{DD}, the modulation index m and all of the saturation voltages $\Delta v_1, \ldots, \Delta v_n$ in the circuit.

In order to minimize the storage capacitance, the bias current or the power consumption we have to select the optimum choice of modulation index and saturation voltages, while still fulfilling the constraints of the circuit.

5.2 Optimization

Often when designing switched current circuits for a specific purpose, we are interested in a circuit that has a specified signal-to-noise ratio SNR, a specified total-harmonic-distortion THD and that is capable of operating at a specified sampling frequency.

At the same time we might be interested in minimizing the storage capacitance, the current consumption or the power consumption.

In this section we will present an optimization methology that can be used for designing switched-current with the above requirements. The optimization methology is presented below.

Methology

The optimization methology is based on noise analysis, as shown in the previous section of this chapter. The steps necessary for carrying out the optimization are shown below.

SNR : Establish an expression for the signal-to-noise-ratio SNR, from which we can derive expressions for the storage capacitance, bias current and power consumption.

Constraints : From the circuit topology we get the constraints, that set a bound on the modulation index m and on the saturation voltages $\Delta v_1, \ldots, \Delta v_n$, for a given supply voltage V_{DD}.

$\{C, m, \Delta v_1, \ldots, \Delta v_n\}$ **:** Using constrained minimization we are able to determine the storage capacitance C, the modulation index m and all of the saturation voltages $\Delta v_1, \ldots, \Delta v_n$.

I **:** The bias current is determined by the settling behavior and by the operating speed of our circuit. The settling behavior is often dictated by the total-harmonic-distortion THD requirements as shown in Chapter 4.

Example 5.2.1
This example will illustrate how the above methology can be used to optimize a cascade connection of two current copiers i.e. a sample delay. We will show the optimization for two different current copiers topologies, a cascode current copier and a folded cascode current copier (see Chapter 2 and Chapter 3) and compare the results.

The constrained optimization of the circuits is performed using the function `CONSTR` found in the optimization toolbox in MATLAB.

Cascode Structure

One of the circuits that we are going to optimize is shown in Fig. 5.5. It consists of a cascade connection of two cascode current copiers forming a sample delay. We immediately notice that each of the current copiers in Fig. 5.5 is the same as the current copier described in the introduction of this chapter.

SNR : Because this sample delay is made from a cascade of two current copier similar to the one described in the introduction of this chapter, we can directly cascade two of the SFG's shown in Fig. 5.4 in order to construct a SFG describing the sampling of the noise sources in the sample delay.

Based on this we immediately see that there is generated three times more noise in the sample delay than in a single current copier. The expression for the SNR is therefore given

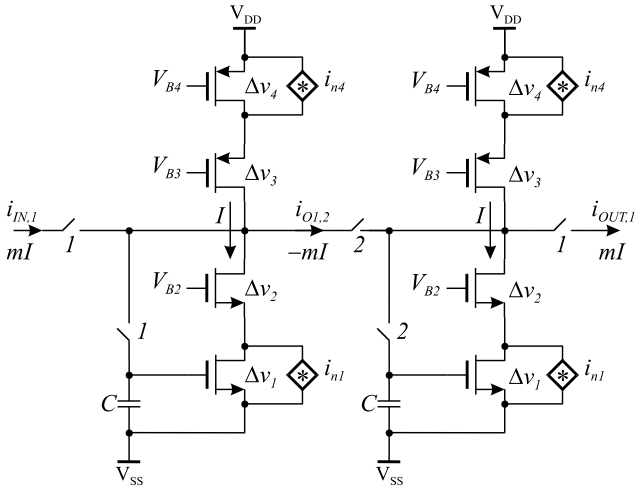

Figure 5.5: Sample delay made from cascading two Cascode Current Copiers

by

$$SNR = \frac{m^2 \cdot \Delta v_1^2}{\frac{48}{3}\frac{kT}{C}\left(1 + \frac{\Delta v_1}{\Delta v_4}\right)} \tag{5.38}$$

Constraints : Before we can optimize the circuit we have to determine the bounds on the variables that we want to optimize. From Fig. 5.5 we see that there are three constraints that must be fulfilled so that the circuit can operate properly.

C-1. $V_{DD} > V_{T_N} + \Delta v_1\sqrt{1+m} + \Delta v_3 + \Delta v_4$

C-2. $V_{T_N} > \Delta v_1\left(\sqrt{1+m} - \sqrt{1-m}\right) + \Delta v_2\sqrt{1+m}$

C-3. $V_{T_N} > \Delta v_2\sqrt{1+m}$

The first constraint is necessary to maintain M3 and M4 in saturation for a full scale input signal. The second constraint bounds the signal swing at the input of the memory transistors so that they stay in saturation. And the third constraint sets a bound on the saturation voltage of the cascode transistors so that it will stay in saturation.

Folded Cascode Structure

One of the circuits that we are going to optimize is shown in Fig. 5.6 and it consists of a cascade connection of two folded cascode current copiers forming a sample delay.

SNR : The overall topology of this circuit is the same as the topology of the cascodet sample delay. Therefore the SFG describing the sampling of the noise sources is the same as the SFG used for the cascode sample delay. The only exception is that the equivalent input noise source is now given by

$$i_{ne} = i_{n1} + i_{n4} + i_{n5} \tag{5.39}$$

We therefore conclude that the expression for SNR of the folded cascode sample delay is given by

$$SNR = \frac{m^2 \cdot \Delta v_1^2}{\frac{48}{3}\frac{kT}{C}\left(1 + \frac{\Delta v_1}{\Delta v_4} + 2\frac{\Delta v_1}{\Delta v_5}\right)} \tag{5.40}$$

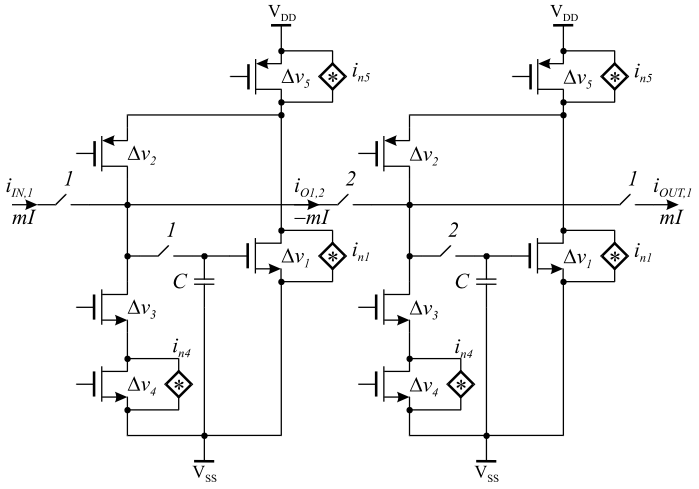

Figure 5.6: Cascade of Folded Cascode Current Copiers

Constraints : Before we can optimize the circuit we have to determine the bounds on the variables that we want to optimize. From Fig. 5.6 we see that there are two constraints that must be fulfilled so that the circuit can operate properly.

FC-1. $V_{DD} > V_{T_N} + \Delta v_1\sqrt{1+m} + \Delta v_2 + \Delta v_5$

FC-2. $V_{T_N} + \Delta v_1\sqrt{1-m} > \Delta v_3 + \Delta v_4$

The first constraint is necessary to maintain M3 and M5 in saturation for a full scale input signal. The second constraint bounds the signal swing at the input of the memory transistors so that the bias transistors M3 and M4 stay in saturation.

Optimization

In the constrained optimization the threshold voltage was set to $V_{T_N} = 0.7V$. Also the lower bound on any saturation voltage was set to $0.15V$.

The constrained minimization showed that the optimum choice for the saturation voltages Δv_2 and Δv_3 was $0.15V$ (the lower bound) independent of the supply voltage i.e. the saturation voltage of the cascoding transistors should be made as small as possible.

Minimizing Storage Capacitance By rearranging the equation for the SNR we get that the storage capacitance for the cascode circuit is given by

$$C = SNR \cdot \frac{48}{3} kT \frac{\left(1 + \frac{\Delta v_1}{\Delta v_4}\right)}{m^2 \cdot \Delta v_1^2} \tag{5.41}$$

and that the storage capacitance for the folded cascode circuit is given by

$$C = SNR \cdot \frac{48}{3} kT \frac{\left(1 + \frac{\Delta v_1}{\Delta v_4} + 2\frac{\Delta v_1}{\Delta v_5}\right)}{m^2 \cdot \Delta v_1^2} \tag{5.42}$$

In Fig. 5.7 we have plotted the minimized storage capacitance for various supply voltages. By increasing the supply voltage we are able to maintain a larger signal swing at storage

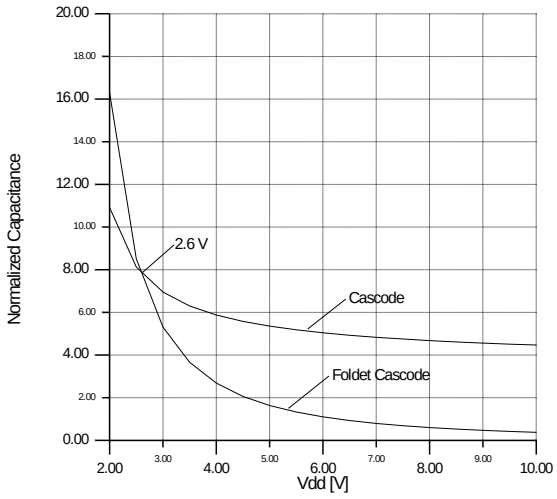

Figure 5.7: Minimized Capacitance dependence on Supply Voltage. The capacitance is normalized with: SNR $\cdot \frac{48}{3}kT$

capacitor, giving an increased SNR. Therefore the storage capacitor is reduced as shown in Fig. 5.7.

At high supply voltages, the storage capacitance of the folded cascode current copier gets somewhat smaller than the storage capacitance of the cascode current copier. The reason for this is that at high supply voltages the voltage swing at the storage capacitor in the cascode CCOP is limited by the threshold voltage V_{T_N} as shown in constraint C-2. This limitation is not found in the folded cascode CCOP.

For both the cascode and the folded cascode CCOP's we se from constraint C-2 and FC-2, that a low threshold voltage V_{T_N} will limit the available signal swing at the storage capacitor, leading to increased power consumption. This is especially true for the cascode CCOP and if designing SI circuits using a low-V_T CMOS process one should consider to use the folded cascode topology.

If however the threshold voltage is reasonably high e.g. around $0.9V$ one should use the cascodet topology at low supply voltages.

At low supply voltages the folded cascode CCOP needs a larger storage capacitor than the cascode CCOP to obtain the same SNR. This is simply because the folded cascode CCOP is more noisier than the cascodet CCOP, se the SNR expressions.

In Fig. 5.8 we have plotted the power consumption for the minimized storage capacitance at various supply voltages. We notice that the power consumption of the folded cascode CCOP is almost independent of the supply voltage, whereas the power consumption of the cascode CCOP increases almost linearly with the supply voltage.

Minimizing Power Consumption By rearranging the equation for the SNR we get that the power consumption for the cascode circuit is given by

$$P_{sup} = V_{DD} \cdot \omega_o \cdot SNR \cdot \frac{48}{3} kT \frac{\left(1 + \frac{\Delta v_1}{\Delta v_4}\right)}{m^2 \cdot \Delta v_1} \tag{5.43}$$

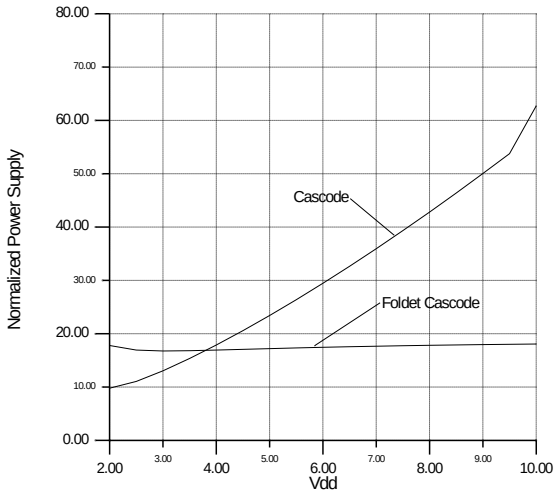

Figure 5.8: Power Consumption for Minimized Capacitance. The power consumption is normalized with: $\omega_0 \cdot \mathrm{SNR} \cdot \frac{48}{3} kT$

and that the power consumption for the folded cascode circuit is given by

$$P_{sup} = V_{DD} \cdot \omega_o \cdot SNR \cdot \frac{48}{3} kT \frac{\left(1 + \frac{\Delta v_1}{\Delta v_4} + 2\frac{\Delta v_1}{\Delta v_5}\right)}{m^2 \cdot \Delta v_1} \tag{5.44}$$

In Fig. 5.9 we have minimized the power consumption for various supply voltages. This figure

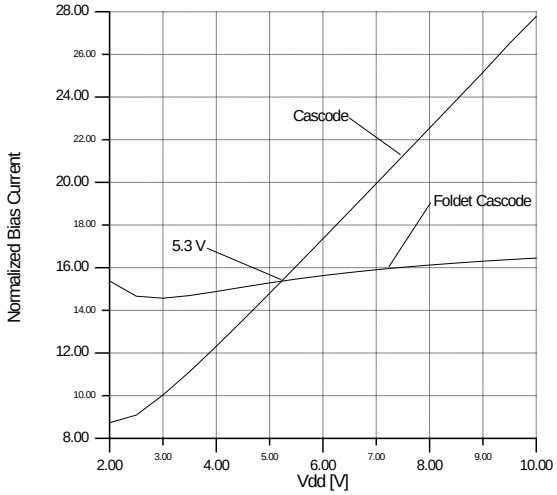

Figure 5.9: Minimized Power Consumption dependence on Supply Voltage. The power consumption is normalized with: $\omega_0 \cdot \mathrm{SNR} \cdot \frac{48}{3} kT$

shows that the folded cascode CCOP has a power consumption that is almost independent of the supply voltage, whereas the power consumption for the cascode CCOP increases almost linearly with the supply voltage.

We notice that the crossing of the cascode and the folded cascode CCOP is around $5.3V$.

In case we are using a low-V_T CMOS process this crossing will decrease drastically making it more feasible to use folded cascode topologies for low-voltage and low-V_T CMOS process.

If however the threshold voltage is reasonably high e.g. around $0.9V$ one should use the cascode topology at low supply voltages.

In Fig. 5.10 we have plotted the storage capacitance for the minimized power consumption at various supply voltages. This figure is similar to Fig. 5.7 which shows the minimized storage capacitance. Again the storage capacitance of the cascode circuit will saturate at a level somewhat higher than the folded cascode circuit.

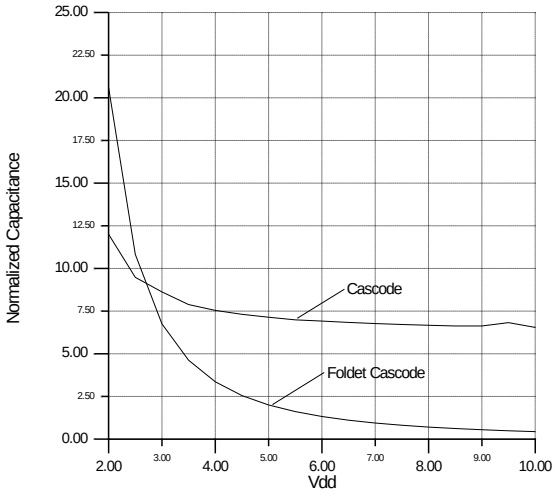

Figure 5.10: Capacitance for Minimized Power Consumption. The capacitance is normalized with: SNR $\cdot \frac{48}{3}kT$

Minimizing Bias Current By rearranging the equation for the SNR we get that the bias current for the cascode circuit is given by

$$I = \omega_o \cdot SNR \cdot \frac{48}{3}kT\frac{\left(1+\frac{\Delta v_1}{\Delta v_4}\right)}{m^2 \cdot \Delta v_1} \tag{5.45}$$

and that the bias current for the foldet cascode circuit is given by

$$I = \omega_o \cdot SNR \cdot \frac{48}{3}kT\frac{\left(1+\frac{\Delta v_1}{\Delta v_4}+2\frac{\Delta v_1}{\Delta v_5}\right)}{m^2 \cdot \Delta v_1} \tag{5.46}$$

In Fig. 5.11 we have minimized the bias current for various supply voltages. For increased supply voltage, the bias current in the folded cascode circuit will decrease, whereas the bias current for the cascode circuit will saturate at a given level. This is due to constraint C-2 found in the cascode CCOP. ■

5.3 Switched Current Circuits Operating in Weak-Inversion

When a MOS transistor is operated in weak-inversion, the square law relationship between gate voltage and drain current is replaced by a exponential relationship much like that for a

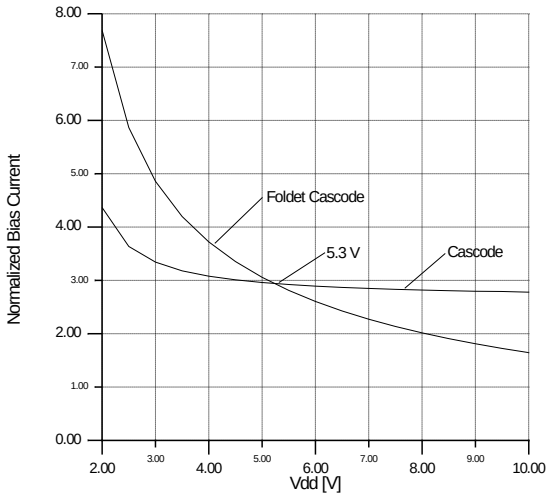

Figure 5.11: Minimized Bias Current dependence on Supply Voltage. The bias current is normalized with: $\omega_0 \cdot \mathrm{SNR} \cdot \frac{48}{3} kT$

bipolar transistor. There is however a major difference between a MOS transistor in weak-inversion and a bipolar transistor and that is that there flows no current into the gate of the MOS transistor in contrast to the base current in the bipolar transistor.

The relationship between the drain current and the gate voltage for a MOS transistor operating in weak-inversion and saturation can be written as

$$i_D = I_{D0} e^{\frac{v_G}{nVt}} \tag{5.47}$$

Also the power spectral density of the white noise in the drain current is given by

$$S_{in}^w = 2kT\frac{g_m}{2} \tag{5.48}$$

In order to investigate the feasibility for switched current circuits operating in weak-inversion we will perform a noise analysis on a simple class A current copier operating in weak-inversion. The structure of this current copier is the same as for the simple current copier described in a previous chapter.

The total power spectral density at the input of the current copier is given as the sum of the power spectral densities of the current source and the memory transistor. We have that

$$S_{in}^w = 2kT\frac{1}{2}(g_{m1} + g_{m2}) \tag{5.49}$$

This noise is in the copy phase, bandlimited by the memory transistor, leading to a sampled white noise with a power spectrum of

$$s_{in}^w = 2kT\frac{1}{2}(g_{m1} + g_{m2}) \cdot \frac{g_{m2}}{2C} = \frac{kT}{C} \cdot \frac{g_{m2}^2}{2} \cdot (1 + \frac{g_{m1}}{g_{m2}}) \tag{5.50}$$

The total power of the sample noise can be found by integrating the power spectrum over the frequency band of interest. Assuming the the we utilize all of the frequency band i.e. $[-f_s/2; +f_s/2]$ we get that the noise power is the same as (5.50) Because the current copier

operates in class A, the input current must be a fraction m of the bias current I. This leads to a signal power of

$$P_{is} = \frac{m^2 I^2}{2} \tag{5.51}$$

The signal to noise ratio (SNR) can now be calculated as

$$SNR = \frac{P_{is}}{P_{in}} = C \cdot \frac{m^2 I^2}{kT\left(1 + \frac{g_{m1}}{g_{m2}}\right) g_{m2}^2} \tag{5.52}$$

From the relationship between the drain current and the gate voltage we have that the small signal transconductance is given by

$$g_m = \frac{I}{nVt} \tag{5.53}$$

If we insert this in the above equation we get that the signal to noise ratio SNR is given by

$$SNR = \frac{P_{is}}{P_{in}} = C \cdot \frac{m^2 V_t^2}{2kT} \tag{5.54}$$

This equation shows that in order to get a large SNR we have to use a very large capacitor because the voltage signal swing is limited by the weak-inversion operation.

The need for a large capacitor C will imply a need for a large transconductance g_{m2} in order keep the bandwidth high to get a proper settling of the current copier.

Therefore the consequence of operating in weak-inversion is that the current consumption will be high and the chip area will be large. This shows that requirements for low-power operation should not dictate the use of weak-inversion switched current circuits.