Part II

Applications

Chapter 6

Switched Current Micropower 4th Order Lowpass/Highpass - Filter

This chapter describes the design and implementation of a 4th order switched current filter. The filter has simultaneous lowpass/highpass outputs, where the cut-off frequencies of the lowpass and the highpass filter are the same. The ratio between the clock frequency and cut-off frequency is equal to 12.58 and the filter has been designed for operation with clock frequencies up to 40kHz. The filter is intended for use in a low voltage and low power environment. Therefore the filter was designed to operate at supply voltages down to $2.0V$.

6.1 Design

When designing a 4th order filter with simultaneous lowpass and highpass output one can choose between several possible topologies.

For instance a 4th order state-variable filter structure can easily realize simultaneous lowpass and highpass filter outputs. There is however one problem concerned with implementing the filter as a single high order state variable filter, and that is a rather high sensitivity towards variations in the filter coefficients [29].

This sensitivity problem is reduced by splitting the filter into a cascade of two 2nd order filter sections (Biquad's) [29]. A general biquad filter section implemented using sample delay's is shown in Fig. 6.1 The transfer function of the filter shown in Fig. 6.1 is easily found

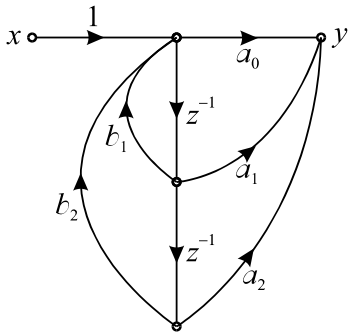

Figure 6.1: Biquad filters section, using sample delays

using Masons formula

$$H(z) = \frac{a_0 + a_1 z^{-1} + a_2 + z^{-2}}{1 - b_1 z^{-1} - b_2 z^{-2}} \tag{6.1}$$

By chosing a butterworth type transfer function for the highpass and lowpass filters we get the following normalized continuos time transfer functions

$$H_{LP}(s) = \frac{1}{s^2 + 1.84775s + 1} \cdot \frac{1}{s^2 + 0.76535s + 1} \tag{6.2}$$

$$H_{HP}(s) = \frac{s^2}{s^2 + 1.84775s + 1} \cdot \frac{s^2}{s^2 + 0.76535s + 1} \tag{6.3}$$

Before we can use these continuos time transfer functions in our switched current filter, we have to make an appropriate frequency transformation from the continuos frequency s to the digital frequency z. For this purpose we have chosen the bilinear s-to-z transformation. given by

$$s_{ct} = \frac{2}{T} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \tag{6.4}$$

Using the relationship $z = e^{sT}$, the above equation can be written as

$$\omega_{ct} = \frac{2}{T} tan(\omega \frac{T}{2}) \tag{6.5}$$

This equation shows that the digital frequency $\omega = 0$ is transformed to the analog frequency $\omega_{ct} = 0$ and that digital frequency $\omega = f_s/2$ (Half the sampling frequency) is transformed to the analog frequency $\omega_{ct} = \infty$.

When designing a digital filter, with a cut-off frequency ω_0, from a normalized analog prototype filter, using the bilinear s-to-z transformation we get that the cut-off frequency ω_0 is transformed to the analog frequency

$$\omega_{ct} = \frac{2}{T} tan(\omega_0 \frac{T}{2}) \tag{6.6}$$

This shows that if we had designed a digital filter by inserting (6.4) into a analog prototype filter we would have got a wrong cut-off frequency. This is because the cut-off frequency of an analog prototype filter is found at $\omega_{ct} = 2\pi \cdot 1$.

In order to get the correct cut-off frequency for the digital filter we have to pre-wrap the frequency transformation (6.4) so that the digital cut-off frequency ω_0 is mapped into the analog frequency $\omega_{ct} = 2\pi \cdot 1$. This is done by dividing (6.4) by (6.6).

Therefore the prewrapped bilinear s-to-z transformation is obtained by replacing the analog frequency s in the analog prototype filter by

$$s = \frac{1}{\psi} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \text{ , where } \psi = tan(\omega_0 \frac{T}{2}) \tag{6.7}$$

The effect of this frequency transformation is that the analog prototype filter is transformed to the digital filter with the following relationship.

$$\frac{1}{s^2 + a_1 s + 1} \longrightarrow \frac{\psi^2(1 + 2z^{-1} + z^{-2})}{(\psi^2 + a_1\psi + 1) - 2(1 - \psi^2)z^{-1} - (a_1\psi - \psi^2 - 1)z^{-2}} \tag{6.8}$$

$$\frac{s^2}{s^2 + a_1 s + 1} \longrightarrow \frac{(1 - 2z^{-1} + z^{-2})}{(\psi^2 + a_1\psi + 1) - 2(1 - \psi^2)z^{-1} - (a_1\psi - \psi^2 - 1)z^{-2}} \tag{6.9}$$

It can be shown that the sensitivity of a biquad filter section implemented using sample delay's can be reduced even further by replacing the sample delays z^{-1} with either a integrator $z^{-1}/(1-z^{-1})$ or a differentiator $(1-z^{-1})$ [6]. The sensitivity properties with a integrator and a differentiator are the same.

We choose to implement the biquad sections using differentiators. When we replace the sample delays with differentiators $D = (1-z^{-1})$ we have to rearrange the filter coefficients $a_0 \dots a_2$ and $b_1 \dots b_2$ in (6.1) accordingly in order to maintain the same transfer function. It is easy to show that the transfer function given by (6.1) is changed to

$$\frac{a_0 + a_1 z^{-1} + a_2 + z^{-2}}{1 - b_1 z^{-1} - b_2 z^{-2}} = \frac{(a_0 + a_1 + a_2) + (a_1 + 2a_2)D + a_2 D^2}{(1 - b_1 - b_2) - (b_1 + 2b_2)D - b_2 D^2} \tag{6.10}$$

Using the above relationship, the bilinear s-to-z transformed analog prototypes can now be implemented using differentiators in the following way

$$\frac{1}{s^2 + a_1 s + 1} \longrightarrow \frac{1 + D + 0.25D^2}{1 - \left(\frac{a_1}{2\psi} - 1\right) D - \left(\frac{a_1}{4\psi} - \frac{1}{4\psi^2} - \frac{1}{4}\right) D^2} \tag{6.11}$$

$$\frac{s^2}{s^2 + a_1 s + 1} \longrightarrow \frac{\frac{1}{4\psi^2} D^2}{1 - \left(\frac{a_1}{2\psi} - 1\right) D - \left(\frac{a_1}{4\psi} - \frac{1}{4\psi^2} - \frac{1}{4}\right) D^2} \tag{6.12}$$

By choosing the ratio between sampling frequency and the cut-off frequency of our lowpass and highpass filters to be $f_s/f_o = 12.58$, we get that the analog prototype filters are transformed into the following digital counterparts.

$$H_{LP}(z) = \frac{1 + D + 0.25D^2}{1 - 2.62135D + 2.28038D^2} \cdot \frac{1 + D + 0.25D^2}{1 - 0.50000D + 3.34105D^2} \tag{6.13}$$

$$H_{HP}(z) = \frac{3.84106D^2}{1 - 2.62135D + 2.28038D^2} \cdot \frac{3.84106D^2}{1 - 0.50000D + 3.34105D^2} \tag{6.14}$$

By utilizing the low sensitivity property of the differentiator based biquad filtersections we will quantize all of the filter coefficients to the nearest multiple of 0.25. This results in the following transfer functions

$$H_{LP}(z) = \frac{1 + D + 0.25D^2}{1 - 2.50D + 2.25D^2} \cdot \frac{1 + D + 0.25D^2}{1 - 0.50D + 3.25D^2} \tag{6.15}$$

$$H_{HP}(z) = \frac{3.75D^2}{1 - 2.50D + 2.25D^2} \cdot \frac{3.75D^2}{1 - 0.50D + 3.25D^2} \tag{6.16}$$

A direct implementation of these transfer functions is shown in Fig. 6.2. By transposing

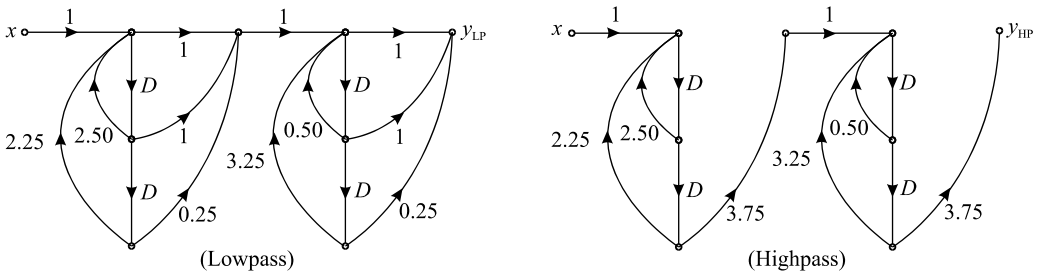

Figure 6.2: SFG for lowpass and highpass filters

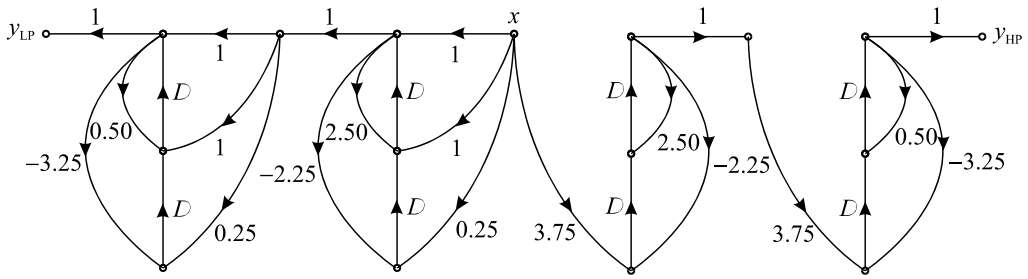

Figure 6.3: Transposed SFG for lowpass and highpass filters.

the SFG's shown in Fig. 6.2, i.e. reversing the flow direction and exchanging the input and outputs, we retain the sensitivity properties [12] and we get a more regular implementation. The SFG for the transposed filters is shown in Fig. 6.3. A Blockdiagram showing the whole filter structure including clock generator, input- and output buffers is shown in Fig. 6.4

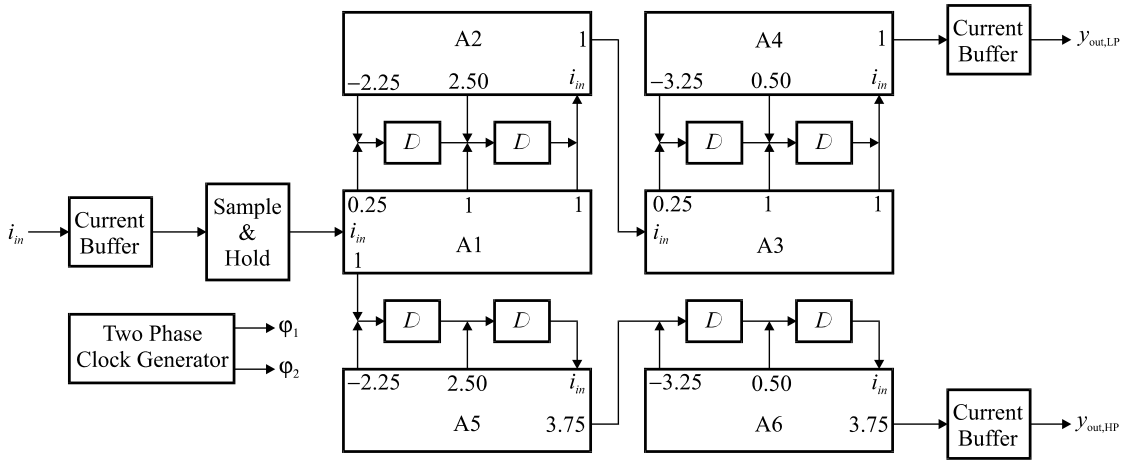

Figure 6.4: Filter Structure based on the transposed SFG

6.2 Implementation

All of the switched current building blocks i.e the differentiators (D) and the Sample and Hold (S/H) are based on the same transconductor. I have chosen the cascode type transconductor (see Chapter 2) because it is relatively simple and it is capable of operating at relatively low supply voltages.

A diagram of the cascode transconductor is shown in Fig. 6.5. I chose to use PMOS transconductor (M1), because it gave a more regular layout of the differentiators with the bias currents that were chosen.

When the transconductor has its input and output short circuited, the input signal current is limited to $\pm I$ and the bias current is set to I/m where m is the modulation index i.e. the fraction of the bias current used for signal swing.

The transconductor is designed so that it can operate at supply voltages down to $V_{DD} = 2.0V$.

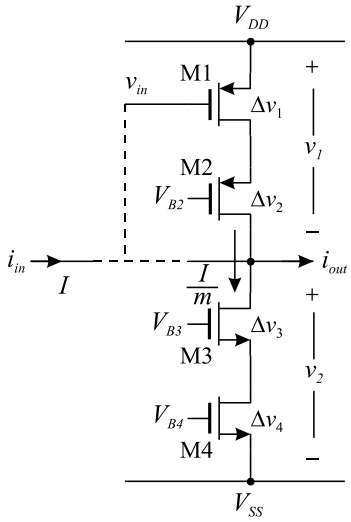

Figure 6.5: Transconductor used in all of the building blocks in the filter

Design of the transconductor: Some of the typical process parameters for the $2.4\mu m$ CMOS process used in this design are shown in Table 6.1. The voltage

Table 6.1: Typical Process parameters for the $2.4\mu m$ CMOS process (MIETEC)

Parameter	*Value*
V_{Tn}	0.9V
V_{Tp}	0.9V
K'_n	$57\mu A/V^2$
K'_p	$17\mu A/V^2$

$$v_{2,min} = \Delta v_3 + \Delta v_4 \tag{6.17}$$

is chosen to be $0.5V$. These $0.5V$ are divided between the transistors $M3$ and $M4$ so that $\Delta v_3 = 0.3333V$ and $\Delta v_4 = 0.1667V$. This implies that

$$v_{1,max} = \Delta v_1\sqrt{1+m} + V_{Tp} = V_{DD} - v_{2,min} = 1.5V \tag{6.18}$$

i.e.

$$\Delta v_1 = 0.6V/\sqrt{1+m} \tag{6.19}$$

Simulations showed that if the modulation index m was chosen close to one, the filter became unstable. This is a direct consequence of the severe settling errors caused by the use of the differentiators (Discussed in the next section of this chapter). Therefore the modulation index m was chosen to $m = 0.5$ implying that the saturation voltage for $M1$ is

$$\Delta v_1 = 0.6V/\sqrt{1.5} = 0.49V \tag{6.20}$$

In order for $M1$ and $M2$ to operate in saturation the following inequality must be fulfilled

$$\Delta v_2 < \frac{V_{Tp}}{\sqrt{1+m}} = \frac{0.9V}{\sqrt{1.5}} = 0.735V \tag{6.21}$$

We therefore choose the saturation voltage of $M2$ to be half the saturation voltage of $M1$ i.e. $\Delta v_2 = 0.245V$.

Because the transconductor operates in class A, the power consumption is determined as the product of the bias current and the supply voltage. In order to get reasonably low power consumption the signal current was chosen to $I = 0.75\mu A$. This implies that the transconductance parameter for M1 is given by:

$$\beta_1 = \frac{2\frac{I}{m}}{\Delta v_1^2} = 12.495\mu A/V^2 \tag{6.22}$$

The above calculations are summarized in Table 6.2, which shows all of the calculated saturation voltages and the peak signal current. All of the circuit parts of the filter use the

Table 6.2: Saturation voltages and the peak signal current used in the transconductor

Saturation voltage	*Value*
Δv_1	0.49V
Δv_2	0.245V
Δv_3	0.1667V
Δv_4	0.3333V
I	$0.75\mu A$
β_1	$12.495\mu A/V^2$

same saturation voltages, as shown in Table 6.2.

6.2.1 Differentiator

The differentiator is the key element in this filter and it is shown in Fig. 6.6. We notice that on clock phase one, the signal at the input of the differentiator is connected directly to the output through the current copier made from transistors $M5, \ldots, M8$ and $M11, \ldots, M14$. The bandwidth of this current copier is determined by

$$\omega_0 = \frac{g_{m5}}{C_{gs5} + C_{gs11}} \tag{6.23}$$

The consequence of this is that there are some severe settling problems found in the filter on clock phase one. By looking at Fig. 6.4 we notice that the on clock phase one, the signal currents have to settle through a chain of four differentiators and one sample and hold circuit.

Assuming that all of these five sections have the same bandwidth, we get that the settling error in the last differentiator is given by

$$\epsilon_5 = e^{-\omega_0 T/2} \sum_{n=0}^{5-1} \frac{(\omega_0 T/2)^n}{n!} \tag{6.24}$$

In order to get a low settling error, we choose $\epsilon_5 = 0.01\%$. This implies that $\omega_0 T/2 = 17.86$. We have chosen that this settling error is found at the sampling frequency $f_{s,max} = 40kHz \sim T = 25\mu S$, therefore the bandwidth of the current copiers is given by $\omega_0 = 1.43MHz$ i.e. the time constant of the current copiers is given by $\tau_0 = 0.7\mu S$.

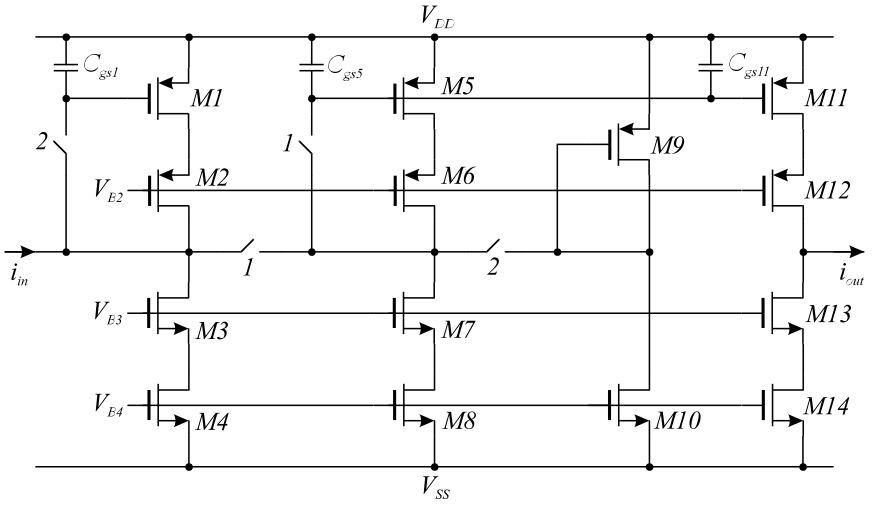

Figure 6.6: Diagram of the differentiator

We are now able to determine the gate-source capacitance necessary to achieve this time constant. We have that the maximum time constant of the current copiers is given by

$$\tau_{max} = \frac{C_{gs}}{g_{m,min}} = \frac{C_{gs}}{\beta_1 \cdot \Delta v_{min}} \tag{6.25}$$

which gives

$$C_{gs} = \tau_{max} \cdot \beta_1 \cdot \Delta v_{min} \tag{6.26}$$

Based on the parameters shown in Table 6.2 we get that the gate-source capacitance is given by

$$C_{gs} = 0.7\mu S \cdot 12.495\mu A/V^2 \cdot 0.49V\sqrt{1-0.5} = 3pF \tag{6.27}$$

The bandwidth of the first current copier, made from the transistors $M1, \ldots, M4$ is chosen to be the same as the bandwidth of the second current copier made from the transistors $M5, \ldots, M8$ and $M11, \ldots, M14$, this implies that:

$$C_{gs1} = C_{gs5} + C_{gs11} \tag{6.28}$$

6.2.2 Sample and Hold

The input signal to the filter chip is a continuos time analog signal current. Before we can perform any filtering of this signal current it has to be sampled and held for a whole clock period, this is required by the differentiators, see Chapter 3.

To perform the sample and hold (S/H) operation a differentiator has been modified to include a switch in series with the input signal current, that operates clock phase two. This arrangement is shown in Fig. 6.7. The effect of placing this extra switch in series with the input signal is that the differentiator is turned into a series connection of two current copiers which will perform the sampling and hold operation.

6.2.3 Current Scaling

The filter coefficients are determined by the current amplifiers $A1, \ldots, A6$ as shown in Fig. 6.3 and Fig. 6.4. When we designed the filter all of the filter coefficients were rounded to the

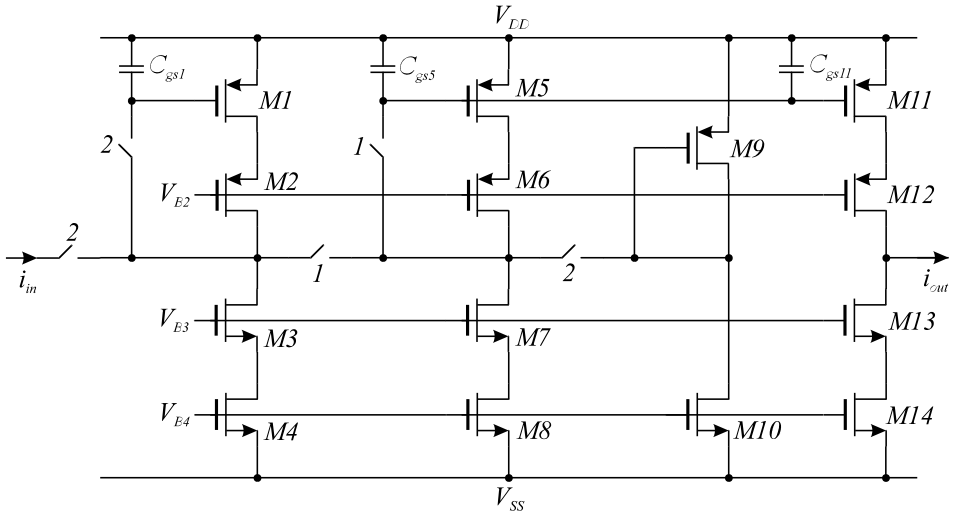

Figure 6.7: Sample and Hold (S/H)

nearest multiple of 0.25. The reason for doing this is that the filter coefficient then easily be implemented, using current mirrors based on unity transistors alone. The use of unity transistors gives us some very accurate filter coefficients (see Chapter F).

The diagram of the current amplifier $A2$ is shown in Fig. 6.8. All of the transconductors

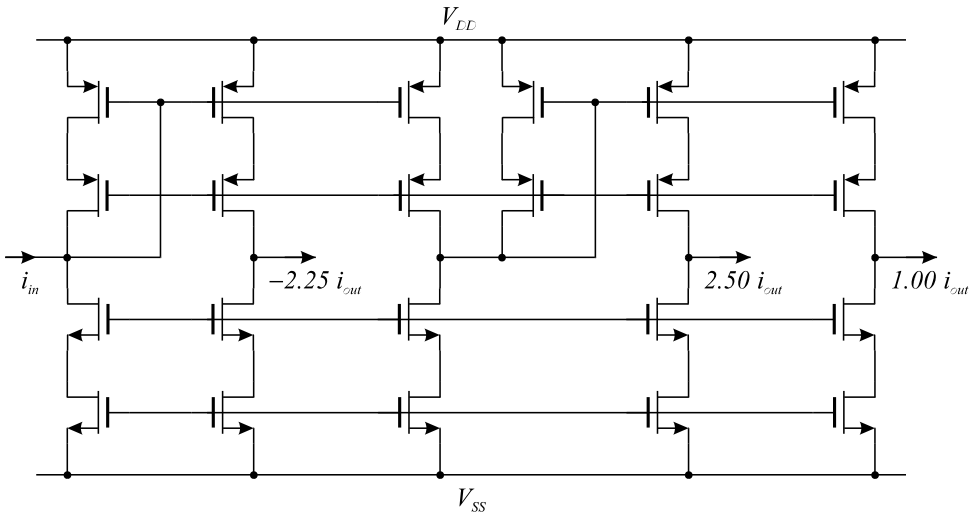

Figure 6.8: Diagram of the current amplifier A2

used in the current mirrors are designed with the saturation voltages listed in Table 6.2 and with a modulation index of $m = 0.5$ i.e. all of the bias currents are two times larger than the peak signal current.

6.2.4 Current Buffer

Current buffers are placed at the input and the outputs of the filter chip. Each of these current buffers contain a set of guard rings and substrate contacts in order to prevent latchup effects.

In Fig. 6.9 we show the diagram of one of the current buffers. In order to assure that

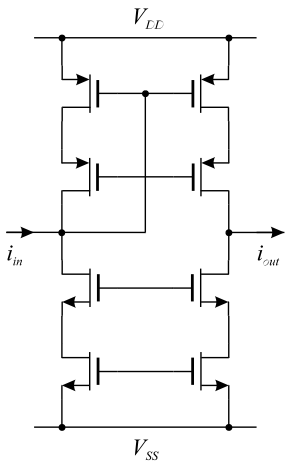

Figure 6.9: Diagram of the Input and Output Buffer

the linearity of the filter is not limited by the current buffers , the modulation index of the current buffer is set to $m = 0.3$ i.e. the transconductors used in the current buffer have a bias current that is tree times larger than the peak signal current.

6.2.5 Two Phase Clock Generator

The two phase non-overlapping clock generator is shown in Fig. 6.10. The clock generator

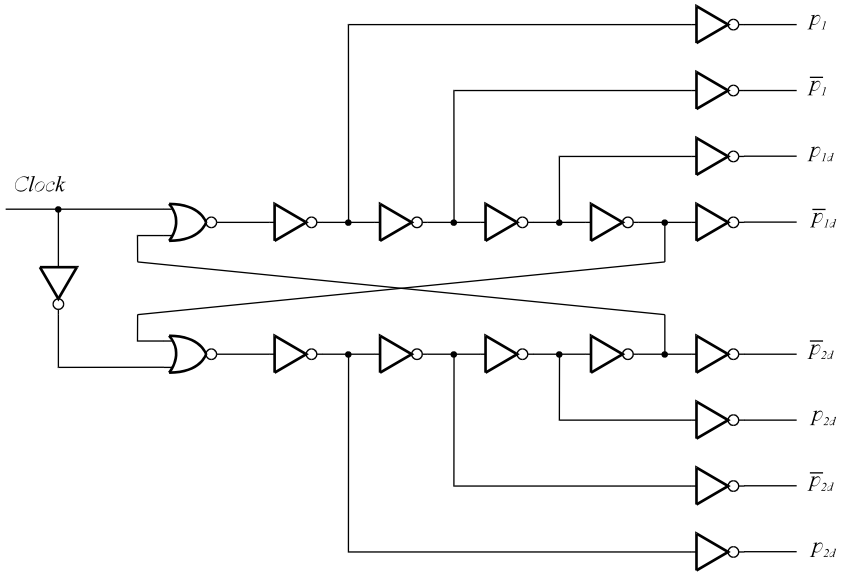

Figure 6.10: Diagram of the Two phase Clock generator

generates from a single clock signal *Clock* two sets of output clock signals. The first set is the phase one clock and the second set is the phase two clock.

Each set has four different clock signals $\{p_1, \overline{p_1}, p_{1d}, \overline{p_{1d}}\}$, where overbar denotes negation and the subscript d denotes delayed. All of these eight clock phases are distributed in a clock

bus to the respective filter units on the chip.

6.3 Layout

The filter chip was implemented in an industry standard analog $2.4\mu m$ CMOS process (MIETEC). All of the Analog and the Digital building blocks were fully custom designed using the Layout editor L-Edit from Tanner Research.

A layout of the whole filter ship is shown in Fig. 6.11. This layout shows the main sections of the chip: Lowpass filter, Highpass filter, Input and Output current Buffers, Bias circuit and the Clock generator.

All of the clock signals are routed in a clock bus between the highpass- and the lowpass filters. The clock signals are routed in Metal 1, and in order to reduce any coupling of the clock signals into the substrate, a grounded Poly 1 plate has been placed beneath the clock bus. Also substrate contacts and guard rings are frequently used, in order to reduce noise coupling. The clock signals are routed so they never cross any analog signal tracks. This is done in order to reduce the coupling of the clock into the signal currents.

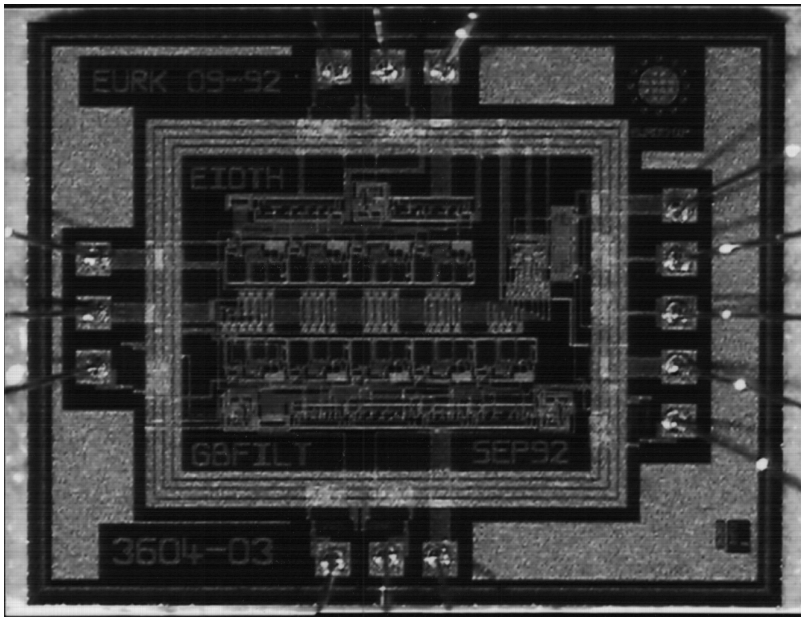

Figure 6.11: Layout of the filter chip

The layout of a single differentiator is shown in Fig. 6.12. This figure shows that the differentiator contains three rather large PMOS transistors.

The first and the largest PMOS transistor performs the differentiation and it has a gate-source capacitance of $C_{gs} = 3pF$. This PMOS transistor corresponds to the transistor M1 shown in Fig. 6.6. The next two PMOS transistor make up a second current copier with an extra current output, this current copier acts as a track and hold for the first current copier, and each one of the PMOS transistors in this current copier has a gate-source capacitance of $C_{gs} = 1.5pF$. These PMOS transistors correspond to the transistors M5 and M11 shown in Fig. 6.6.

The layout of current amplifier A_2, is shown in Fig. 6.13. All of the current amplifiers are a bunch of cascade connections of current mirrors, with different scaling factors. In order

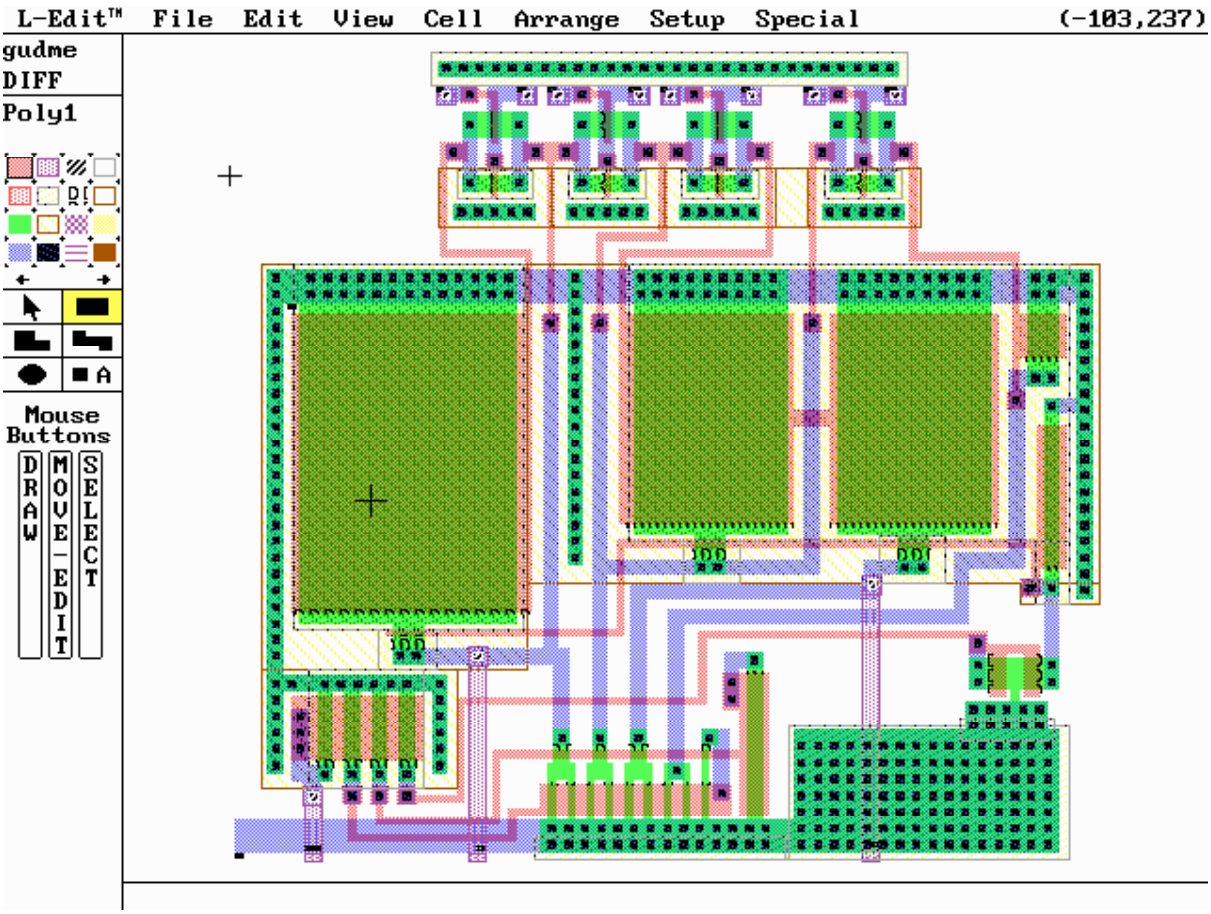

Figure 6.12: Layout of a differentiator

to achieve precise scaling, unity transistors have been used in all of the current mirrors, as shown in Fig. 6.13.

6.4 Experimental Results

A MPW prototype of the filter chip was made and measurements showed that the filter was capable of operating at supply voltages down to $2V$ and with a total supply current of $211\mu A$ at a sampling frequency of 50kHz.

Measurements also showed that the filter operated correctly with clock frequencies up to 50kHz and with a ratio of 12.5 between the sampling frequency and the cut-off frequency.

The area of the chip core is $1.33mm^2$ of which the lowpass filter occupies $0.57mm^2$ and the highpass filter $0.46mm^2$.

6.4.1 Frequency Response

The frequency response of the filter chip was measured at different supply voltages and with different clock frequencies.

In Fig. 6.14 and Fig. 6.15 the filter is operating with a sampling frequency $f_s = 25kHz$ at the supply voltages $V_{DD} = 2.0V$ and $V_{DD} = 3.3V$.

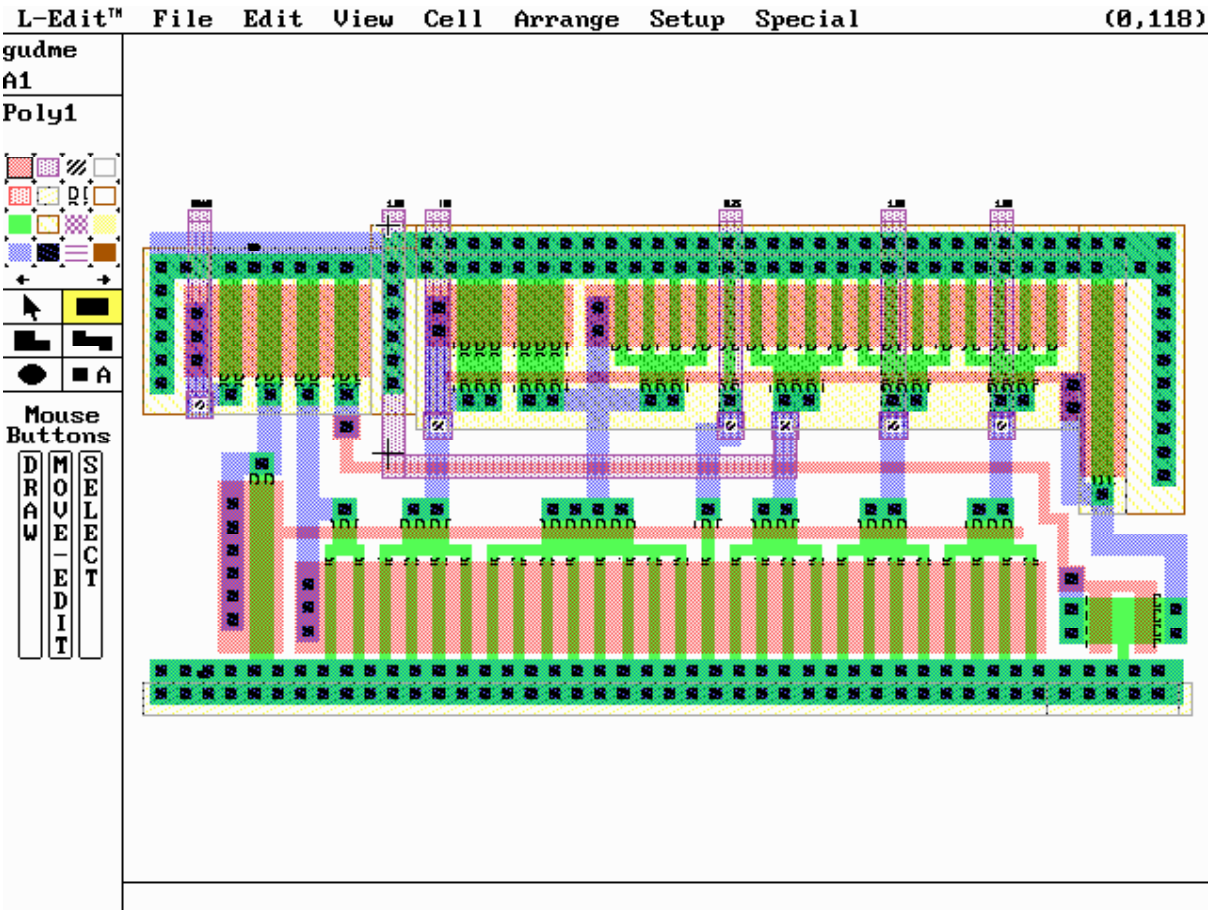

Figure 6.13: Layout of the current amplifier A2

These figures show that the cut-off frequency of the lowpass and the highpass filters are the same and that the cut-off frequency is approximately $f_o = 2kHz$. This gives an approximate ratio between sampling frequency and cut-off frequency off $f_s/f_o = 25/2 = 12.5$. The filter was designed so that this ratio should be 12.58. At a sampling frequency of $f_s = 25kHz$ this should give a cut-off frequency off $f_o = 1.987kHz$. So we see that the measured and the expected cut-off frequency agree very well.

We also notice that for the lowpass filter, the noise floor is approximately $62dB$ below the signal level, and for the highpass filter, the noise floor is approximately $47dB$ below the signal level.

In Fig. 6.16 and Fig. 6.17 the filter is operating with a sampling frequency $f_s = 50kHz$ at the supply voltages $V_{DD} = 2.0V$ and $V_{DD} = 3.3V$.

These figures show that the cut-off frequency of the lowpass and the highpass filters are the same and that the cut-off frequency is approximately $f_o = 4kHz$. This gives an approximate ratio between sampling frequency and cut-off frequency off $f_s/f_o = 50/4 = 12.5$. The filter was designed so that this ratio should be 12.58, at a sampling frequency of $f_s = 50kHz$ this should give a cut-off frequency off $f_o = 3.975kHz$. Again we notice that there is a very good agreement between the measured and the expected cut-off frequency.

We also notice that for the lowpass filter, the noise floor is approximately $54dB$ below the signal level, and for the highpass filter, the noise floor is approximately $47dB$ below the

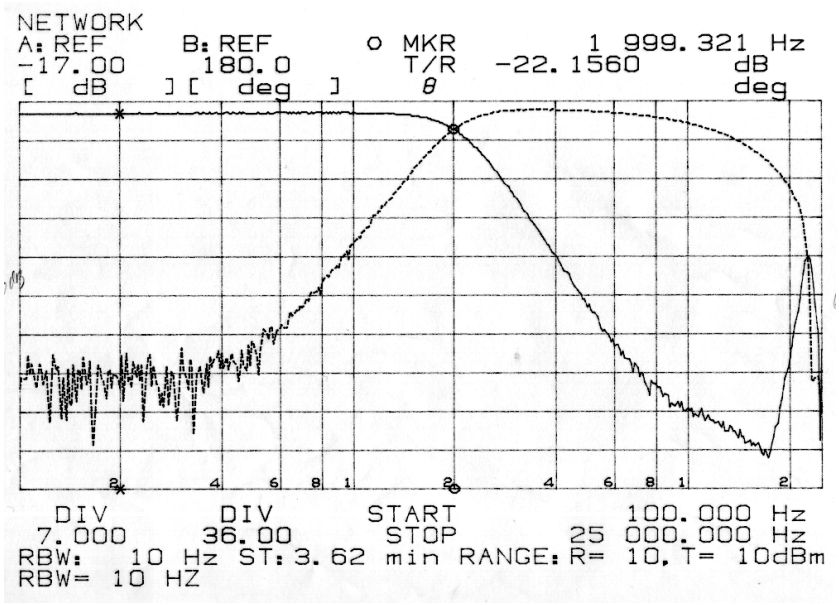

Figure 6.14: Frequency response with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 2.0V$

signal level.

6.4.2 Noise Floor

The noise at the lowpass and the highpass filter outputs, with no input signal, was measured at two different sampling frequencies.

Lowpass output

In Fig. 6.18 and Fig. 6.19 we have the noise at the lowpass output at the sampling frequencies $f_s = 25kHz$ and $f_s = 50kHz$. We notice that the noise has a lowpass shape that is similar to the lowpass frequency response shown previously. We also notice that the noise level at the sampling frequency $f_s = 50kHz$ is a little bit lower than the noise level found at the sampling frequency $f_s = 25kHz$. Theoretically the difference should be $3dB$ because the noise power in the frequency band $[-f_s/2; +f_2/2]$ is independent of the sampling frequency.

Highpass output

In Fig. 6.20 we have the noise at the highpass output at the sampling frequencie $f_s = 25kHz$. We notice that the shape of the noise at the highpass output is similar to the shape of the noise at the lowpass output.

6.5 Conclusion and Future Work

This chapter has described the design, implementation and measurements of a 4th order lowpass and highpass filter. The lowpass and highpass filters were designed for low sensitivity and then optimized for low voltage and low power operation.

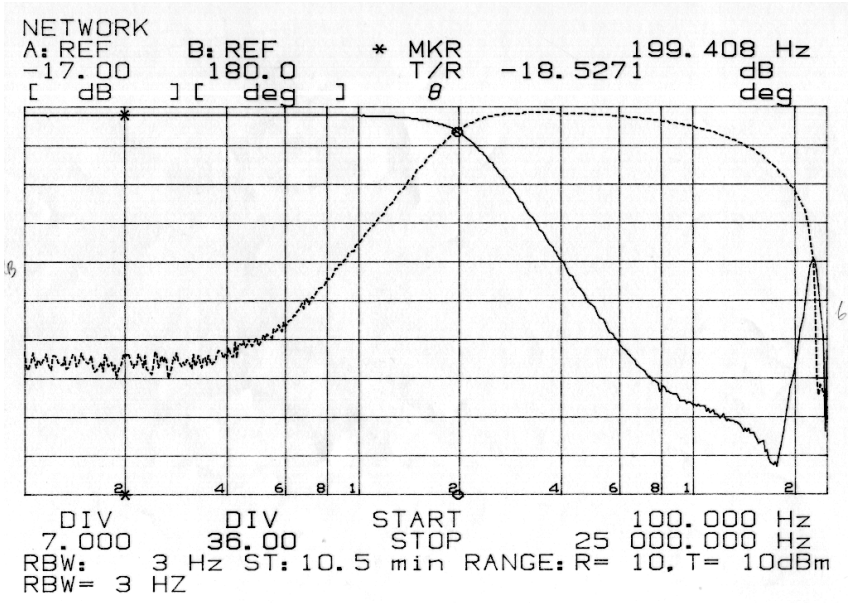

Figure 6.15: Frequency response with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 3.3V$

This chapter has also demonstrated that using the switched current technique it is possible to design high order lowpass and highpass filters using relatively simple circuit configurations. All of the circuits used in this filter rely solely on the use of cascode PMOS transconductors.

Measurements showed that the noise performance of the lowpass and the highpass filters was not too good. This is partly due to the fact that noise analysis was not taken into account when the filters were implemented. Another limiting factor on the noise performance is the severe settling problems found in this particular design. Because the filters are based on differentiators we have previously discussed that the signals have to settle throughout the whole filter on clock phase one. This of course introduces some stability problems that forced us to limit the modulation index m to 0.5. This rather low modulation index contributes largely to the rather poor noise performance.

In case this filter should be re-designed for better noise performance, the differentiators should be replaced by sample delay integrators (see Chapter 3). By using integrators the signal currents only have to settle internally in each integrator and not throughout the whole filter. This would eliminate all of the settling problems and make it possible to increase the modulation index m so that it comes closer to one. This in turn will increase the signal-to-noise-ratio SNR.

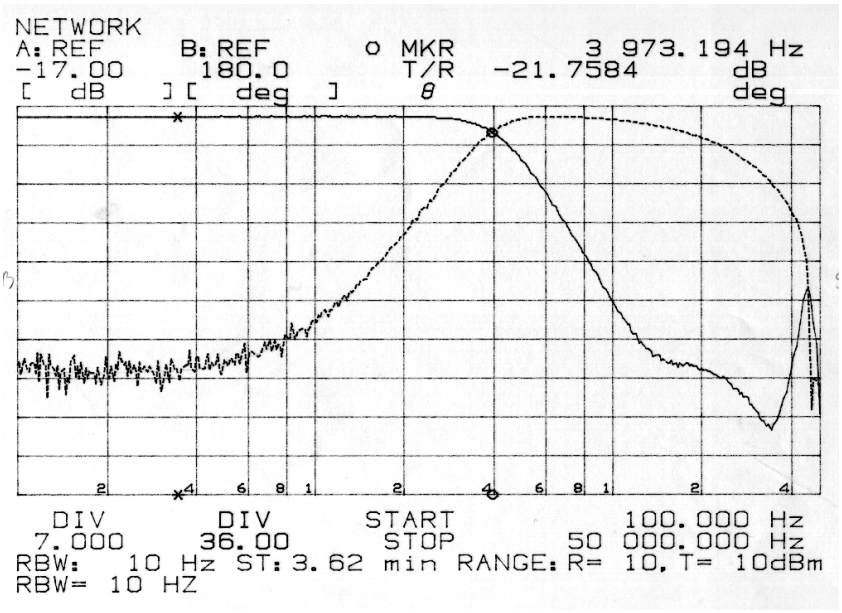

Figure 6.16: Frequency response with a sampling frequency of $f_s = 50kHz$ and at a supply voltage of $V_{DD} = 2.0V$

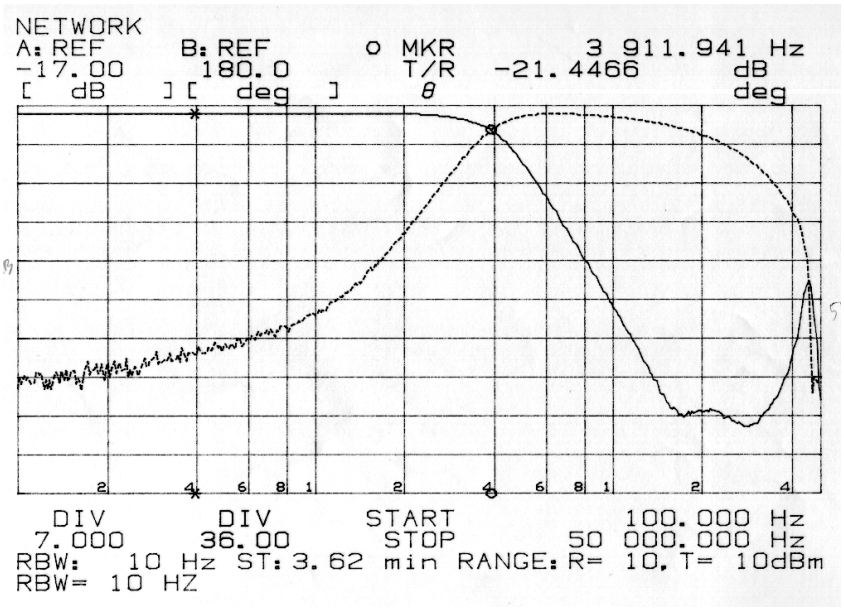

Figure 6.17: Frequency response with a sampling frequency of $f_s = 50kHz$ and at a supply voltage of $V_{DD} = 3.3V$

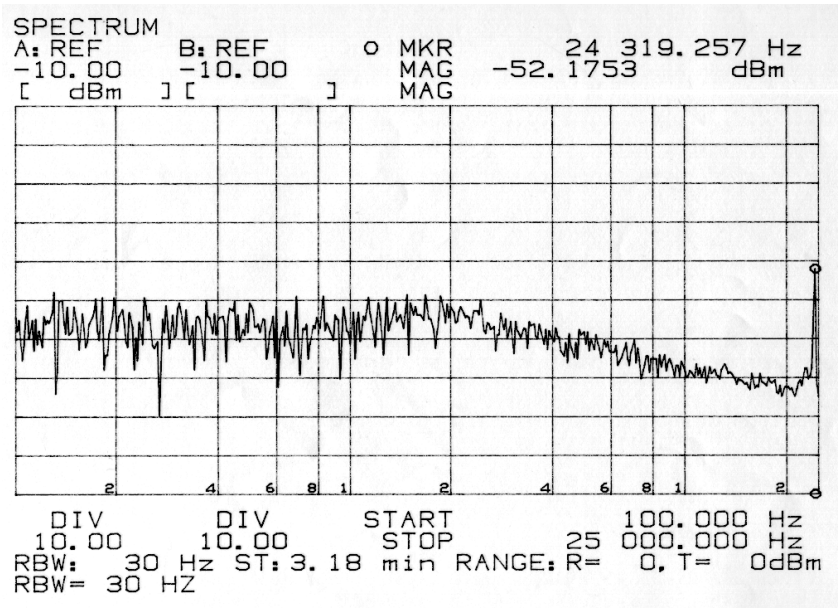

Figure 6.18: Lowpass output noise with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 2.0V$

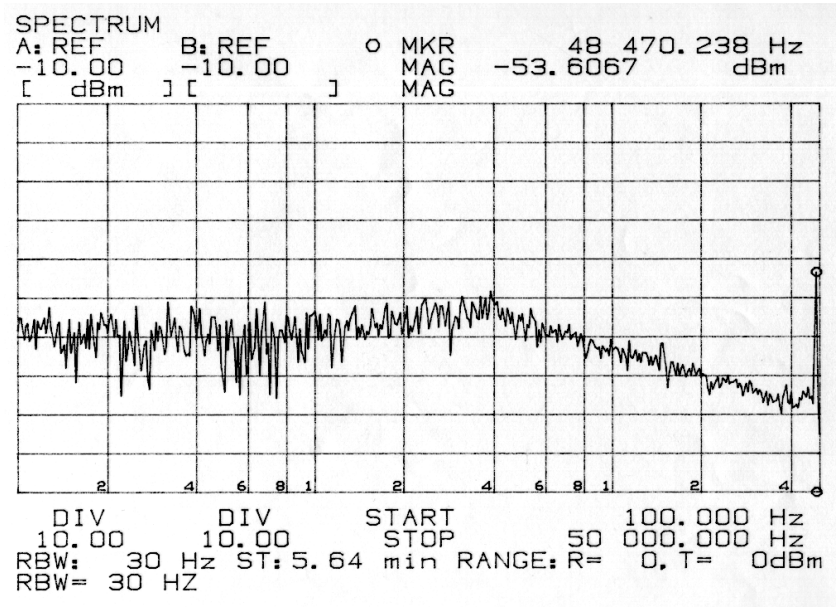

Figure 6.19: Lowpass output noise with a sampling frequency of $f_s = 50kHz$ and at a supply voltage of $V_{DD} = 2.0V$

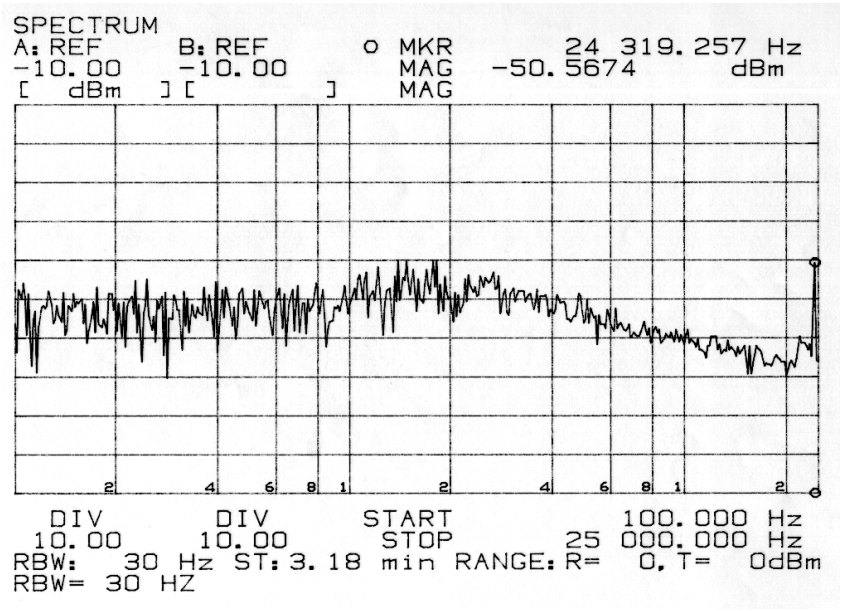

Figure 6.20: Highpass output noise with a sampling frequency of $f_s = 25kHz$ and at a supply voltage of $V_{DD} = 3.3V$