Chapter 8

Serial A/D and D/A Converter

This chapter describes a new singleturn potentiometer with digital output that is to be used in the volume control of a hearing aid amplification system. Traditionally the slide potentiometer has been used as the volume controlling device. However, the lifetime of this component is rather limited. This is due to the galvanic contact between the metalpointer and the carbon slide combined with the hostile and humid environment in which the component has to function. This makes it profitable to look for an alternative to this component.

8.1 Introduction

The main idea behind the new component is to let magnetic sensitive transistors (MAGFET's) on a silicon chip detect the position of a movable bar magnet as shown by Figure Fig. 8.1. In this way there will be no galvanic contact between the anglesetting device and the electrical circuit, and the lifetime of the component will be increased significantly. An iron disk is placed beneath the chip to increase the magnetic field applied to the MAGFET's. The MAGFET is a multiple drain terminal transistor capable of giving a differential output current proportional to the magnetic field applied to it.

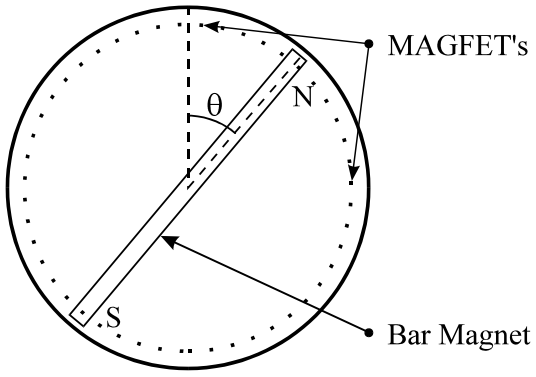

Figure 8.1: Basic configuration of the Angledetecting system

The size of the magnetic field that will be applied to a MAGFET on the chip is a rather complex function of the angle and the dimensions of the bar magnet, the placement of the MAGFET's and the chosen magnetic material. Simulations based on the 'finite element'-method [33] indicates that the magnetic flux through a MAGFET placed at $\theta = 0°$ approximately can be expressed as a cosinusoidal function of the angle of the bar magnet θ (see

Fig. 8.2).

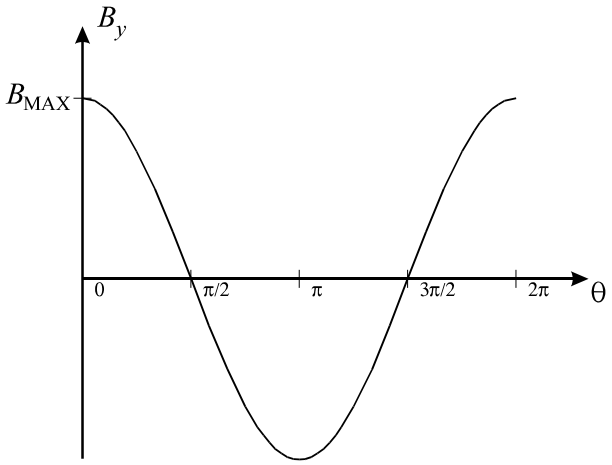

Figure 8.2: Approximate *Angle to Magnetic flux* transfer function

It is obvious that the output from this one MAGFET alone will not be enough for detecting any angle between 0° and 360° unambiguously. Therefore a multiple MAGFET solution is necessary. Two different solutions described in the next two sections have been proposed [34].

8.1.1 The "Digital" solution

In the first solution called the "digital" solution 2^n MAGFET's lie equally spaced on the circle. By finding the MAGFET with the largest positive output one could find the angle position of the MAGFET and represent it with a n-bit digital number. However, the offset errors of the MAGFET's are found to be quite large compared to the maximum available signal current and an offset compensation of every MAGFET is necessary to ensure a linear *Angle to digital output* transfer function. There will be only four terminals on the chip and no room for external components (except for a capacitor for stabilizing the supply voltage) so the offset compensation has to be implemented as a permanent storage on the chip. The large amount of MAGFET's ($2^7 = 128$) to be compensated makes this solution difficult to realize. An implementation containing as few MAGFET's as possible is to prefer.

8.1.2 The Analog solution

Instead of comparing a large number of MAGFET's to get the digital output number directly, one could implement the "potentiometer" with only two MAGFET's as shown in Figure Fig. 8.3.

Based on the assumption that the differential output current from a MAGFET is a linear function of the magnetic field applied to it, the currents available for angledetection are shown in Fig. 8.4.

From this Figure it is clear that any angle position unambiguously can be detected. When generating a 7-bit digital number the two most significant bits (MSB) can be determined by simply reading the signs of the two MAGFET currents[1], and the third MSB can be provided

[1]This will divide the input angle into four equally sized intervals which can be represented by the two most significant bits

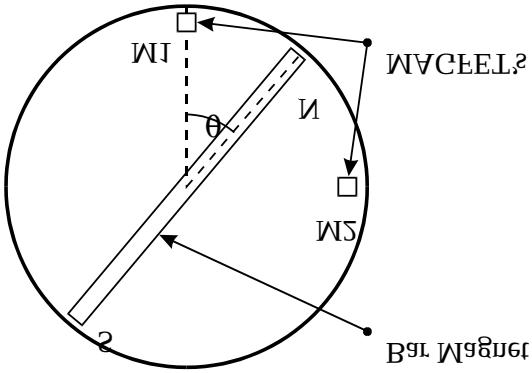

Figure 8.3: 'Two MAGFET' implementation

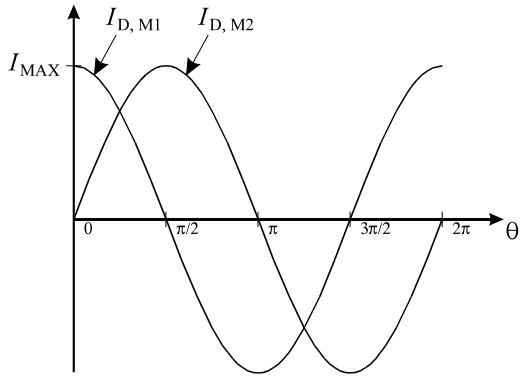

Figure 8.4: The MAGFET signal currents

by comparing the two currents numerically, $|I_{D,\mathrm{M1}}| > |I_{D,\mathrm{M2}}|$. The four least significant bits can be generated by A/D-converting the numerical smallest current with the numerical largest current as a reference. This is in effect a division expressed by (8.1).

$$4\ \mathrm{LSB} = f_{DEC}(D_3D_2D_1D_0) = \frac{\min\{|I_{D,\mathrm{M1}}|, |I_{D,\mathrm{M2}}|\}}{\max\{|I_{D,\mathrm{M1}}|, |I_{D,\mathrm{M2}}|\}} \tag{8.1}$$

The f_{DEC} function indicates that a decoding of the result is taking place. Simulations on the transfer function of the system indicate that an approximate linear *Angle to digital output*-transfer function indeed is achievable with a appropriate choice of dimensions and placement of the bar magnet and the MAGFET's and magnetic material. The simulations were based on the 'finite element' analysis method using the `ANSYS` program [33]. The optimal dimensions of the bar magnet in terms of good linearity was found to be 0.5 mm × 0.65 mm × 2 mm (HWL). The MAGFET was found to be exposed to a magnetic field in the range of ±0.25 T.

8.2 The SI A/D – D/A System

This section contains a description of the entire system for offset measuring and compensating MAGFET's and for decoding output signals from the two MAGFET's.

8.2.1 Introduction

In order to make a correct position detection of the bar magnet the system must meet several specifications. The A/D – D/A system must be able to measure the offset error by an 8 bit A/D-conversion, make a permanent digital storage of the offset error and make a D/A-conversion of the stored error and subtract it from the MAGFET current. The measuring and storing has to be done without any magnetic signal applied to the MAGFET, i.e. before the bar magnet is placed on the top of the chip. The D/A-conversion and the subtraction of the stored error from the MAGFET current must be carried out before any processing on the MAGFET currents can take place. Additionally the system must be able to detect the signs of the MAGFET currents and to compare the two MAGFET currents for generating the three most significant bits in the output. A division of the two MAGFET currents must be carried out for generating the four least significant bits and a decoding of the seven bit number for ensuring a linear *Position Angle to Output* function must take place. The specifications are listed in short form below.

- 8 bit A/D conversion of the offset current of each MAGFET
- Permanent Digital storage of the offset errors represented by a 8 bit number
- 8 bit D/A conversion of the stored errors
- Compensation of offset errors (in terms of subtraction of currents)
- Detection of sign of currents
- Comparison of the two MAGFET currents
- Division of the two currents with a 4 bit digital output
- Decoding the digital output

The specifications will be analyzed in detail in the following sections and implementations of circuitry will be presented.

The A/D conversion

The digital output signal of the A/D converter (ADC) is not to be processed in any way except of the storage and following D/A conversion. To make use of this fact, it is advantageous to implement the ADC utilizing the *successive approximation method* that makes use of a D/A converter (DAC) [35, pp. 651–652]. By using the same DAC both in the D/A conversion and in the A/D conversion unwanted nonlinearities in the DAC will be cancelled out. Also it is an efficient solution in terms of minimizing area.

Permanent digital storage

The permanent digital storage will be implemented using an E^2PROM technology. In this project so far we had no access to a such technology so all internal storage have been carried out using standard RAM technology.

4 bit division

Because of the digital output the division can by carried out as an ratiometric A/D conversion with the nominator as reference and the denominator as the input. Therefore it will be most convenient if the A/D converter is implemented with a current source as reference for converting the current input.

Detection of signs and comparement of currents

In a *successive approximation* A/D system capable of converting currents into digital numbers a current comparator is necessary. This comparator will be used for detection the signs of the MAGFET output currents giving us the two *most significant bits* (MSB). The 3. MSB is generated by comparing the two MAGFET output currents. This can be done by simply subtracting the two currents numerically and apply the result to the comparator $|I_{D,M1}| - |I_{D,M2}| > 0$?

The D/A conversion

The D/A converter can be implemented utilizing the *current scaling method*. This can be done with a resistance network (ex. R – 2R – chain) or a current mirror network scaling a reference current into currents that can represent the weighted bits (MSB, . . . , LSB) [35, pp. 623–629]. This implementation is quite fast but unfortunately with a large use of area. The method rely on a tight matching between the large number of components that give rise to a large use of area. The nonmonotonic property of this type of DAC deteriorates the dynamic range and therefore the *effective* number of bits.

A less area consuming alternative is to implement the DAC following a serial algorithm. By converting the MSB first and the LSB last it is possible to leave out the *successive approximation register* in the A/D conversion. A such serial DAC has been implemented in *switched current* technique [24] and the whole A/D – D/A system is described in the following sections.

8.2.2 Operation of the A/D – D/A system

This section gives a description of the operation of the A/D – D/A system and in the next section we will see how it is used to both offset compensate MAGFET's and to determine the angle position of the bar magnet.

In Figure Fig. 8.5 we have a block diagram of the A/D – D/A conversion system. From this block diagram we see that it consists of a staircase generator, that generates a sequence of exponentially decaying current pulses, an accumulator, that is capable of accumulating the current pulses from the staircase generator, a current comparator a D–flip flop (D–FF) and some registers and a control unit. The system can be made to operate both as a successive approximation A/D converter and as a serial D/A converter. We will now describe how this can be done and at the same time show that the same hardware can be used to implement the A/D conversion and the D/A conversion, which of course makes the system very compact.

Operation as A/D Converter

When the system is setup to operate as a successive approximation A/D converter (Mode 1 and 2) all of the building blocks of Figure Fig. 8.5 are utilized. The staircase generator is generating a sequence of MSB followed by 2nd MSB etc. ending with LSB. When the output is MSB the output of the accumulator (MSB as well) is subtracted from the input

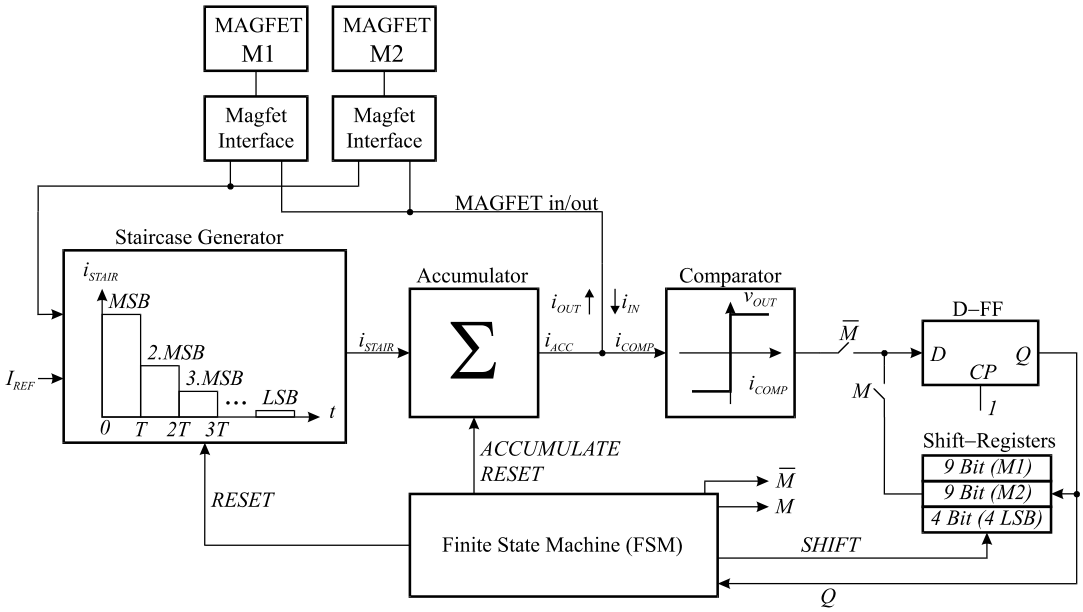

Figure 8.5: Block diagram of the A/D – D/A system

current that is to be converted and the sign of the resulting current is shown on the output of the comparator. This sign signal is both shifted into the shift register and passed to the control unit, and depending on the sign the control unit decides whether the accumulator should accumulate the output from the staircase generator (sign is positive) or not (sign is negative). The same scheme now is repeated for 2nd MSB and so on, and the staircase outputs are only accumulated when the output of the comparator is positive. The digital number representing the input current is now stored in the shift register and is ready for D/A-conversion.

Expressed in detail the following things happen. The control signal (M) is brought low which enables the input current, i_{IN}, that is to be converted. The accumulator and the staircase generator are cleared (RESET) and a reference current, I_{REF}, is applied to the staircase generator. The first current pulse from the staircase generator, $a \cdot I_{REF}$, is passed through the accumulator and subtracted from the input current, i_{IN}. The difference, $i_{IN} - a \cdot I_{REF}$, is sensed by the current comparator which generates a high or a low output that is latched by the D–flip flop (D–FF). If $i_{IN} - a \cdot I_{REF} > 0$ then Q = 1 else Q = 0. The Q output is now shifted into the shift register and the accumulator accumulates the current, $Q \cdot a \cdot I_{REF}$. The shift register will now contain the first bit, (D1). The next current pulse from the staircase generator, $a^2 \cdot I_{REF}$, is passed through the accumulator and is subtracted from the input current, i_{IN}, together with the already accumulated current. The difference, $i_{IN} - (D1 \cdot a \cdot I_{REF} + a^2 \cdot I_{REF})$, is sensed by the current comparator etc. and we have now generated the next bit, (D2). The shift register now contains the sequence (D2,D1). Continuing this operation for n clock cycles forces the shift register to contain the sequence $(Dn, Dn\text{–}1, \ldots, D2, D1)$ which corresponds to the current, $I_{REF} \cdot a \cdot (D1 + D2 \cdot a + \cdots + Dn \cdot a^{n-1})$. If $a = 0.5$ we have a linear conversion of the input current, i_{IN}, to the binary figure $(Dn, Dn\text{–}1, \ldots, D2, D1)$.

Operation as D/A Converter

When the system is set up to operate as a serial D/A converter the operation of the staircase generator and the accumulator is the same as in A/D mode but the comparator is not used. Instead the "sign signal" now is shifted out from the shift register to control the accumulation. The resulting output of the accumulator is now subtracted from the uncompensated MAGFET current and stored in a current copier.

Expressed in detail the following things happen. The control signal (M) is brought high which enables output from the accumulator, i_{OUT}. The accumulator and the staircase generator are cleared (RESET) and a reference current, I_{REF}, is applied to the staircase generator. The first current pulse from the staircase generator, $a \cdot I_{REF}$, is passed through the accumulator and the shift register is shifted one bit through the D–FF. The control unit then receives the first bit (D1) and uses it to control the accumulator so the accumulator will accumulate the current, $\mathrm{D1} \cdot a \cdot I_{REF}$. The next current pulse from the staircase generator, $a^2 \cdot I_{REF}$, is passed through the accumulator and the shift register is shifted one bit through the D–FF. The control unit then receives the next bit (D2) and uses it to control the accumulator so the accumulator will accumulate the current, $\mathrm{D2} \cdot a^2 \cdot I_{REF}$. Continuing this for n clock cycles forces the accumulator to contain the current, $I_{REF} \cdot a \cdot (\mathrm{D1} + \mathrm{D2} \cdot a + \cdots + \mathrm{D}n \cdot a^{n-1})$, which corresponds to the originally A/D converted current.

Offset Compensation and Position Detection

The system is controlled by a finite state machine realized with a PLA. It works in two different modes. In Mode 1 the two offset currents is measured (A/D-converted) and stored digitally. In Mode 2 the stored error signals are D/A-converted and subtracted from the MAGFET currents and the position of the bar magnet is determined from the two offset compensated MAGFET currents. The signal (M) of Figure Fig. 8.5 determines which of the two modes the system should follow and it will be set from outside the chip. The sequences of the two modes are shown schematically below

Mode 1 : Storage of offset errors (No magnetic signal applied)

1. 8 bit A/D-conversion of $I_{\mathrm{M1,OFF}}$
2. Storage of $I_{\mathrm{M1,OFF}}$
3. 8 bit A/D-conversion of $I_{\mathrm{M2,OFF}}$
4. Storage of $I_{\mathrm{M2,OFF}}$

Mode 2 : Position detection (Magnetic signal applied)

1. 8 bit D/A-conversion of $I_{\mathrm{M1,OFF}}$; $I_{\mathrm{M1,SIGNAL}} = I_{\mathrm{M1}} - I_{\mathrm{M1,OFF}}$
2. 8 bit D/A-conversion of $I_{\mathrm{M2,OFF}}$; $I_{\mathrm{M2,SIGNAL}} = I_{\mathrm{M2}} - I_{\mathrm{M2,OFF}}$
3. $I_{\mathrm{M1,SIGNAL}} > 0$? ; $I_{\mathrm{M2,SIGNAL}} > 0$? ; $|I_{\mathrm{M1,SIGNAL}}| > |I_{\mathrm{M2,SIGNAL}}|$? $\Rightarrow$ 3 MSB
4. 4 bit A/D-conversion : $\frac{\min\{|I_{D,\mathrm{M1}}|,|I_{D,\mathrm{M2}}|\}}{\max\{|I_{D,\mathrm{M1}}|,|I_{D,\mathrm{M2}}|\}}$ $\Rightarrow$ 4 LSB

In the two 8 bit A/D conversions of Mode 1 the reference current is generated by a separate current source. The input current is the offset current from MAGFET M1 in the first conversion and the offset current from MAGFET M2 in the second conversion. In the 4 bit A/D conversion of Mode 2 the reference current is the numerically larger of the two

MAGFET currents and the input current is the numerically minor of the two MAGFET currents. This gives us a digital output equal to (8.1).

In the 8 bit D/A conversions of Mode 2 the output current of the accumulator, equal to the offset current of the MAGFET to be compensated, is subtracted from the MAGFET output current. The resulting current, which is the MAGFET signal current proportional to the magnetic field, is then stored in a current copier and is ready for further processing.

The MAGFET only has to be turned on for one clock cycle for measuring the MAGFET current (See Section 8.2.3). The operating clock frequency for the switched current system is 25 kHz. An angledetection has to be done at every 100 ms meaning that the *turn on*-dutycycle for the MAGFET is less than 0.1 %. The circuit has been optimized to work with a supply voltage of 2.2 V and has a static current consumption of 10 μA. The total process of Mode 2 is carried out in 32 clock cycles making the *turn on*-dutycycle for the entire circuit (including all digital operations) less than 2 %.

8.2.3 Analog building blocks

In this section the operation of the analog building blocks are described in detail.

The current copier

To make the A/D – D/A conversion system compatible with standard digital CMOS technology and to make use of the fact that the signals we have to operate with are currents we decided to implement all the analogue functions in *switched-current techniques* [24]. This implies that the analogue functions will rely heavily on the use of current copier cells. A current copier cell is basically built from an inverting transconductor a capacitor for storage and from switches to control the operation. Fig. 8.6 shows the transistor diagram of the transconductor that has been used in the current copier cells in this A/D – D/A conversion system. The reason for using this transconductor in this design is that it is capable of operating at relatively low supply voltages and with reasonably good accuracy [25, 24, 36]. When used in a current copier the signal is stored on the gate-source capacitor, C_{gs}, of M1. M2 is used to cascode M1 so that we get reduced channel-length modulation and a lower capacitive coupling from the output node to the input node. M3 and M4 make up a cascodet current source. The signal currents that are handled by the A/D – D/A converter system are in the order of 1 μA, therefore the bias currents in the current copier cells are also in this order of magnitude. To get small kT/C noise in the current copier cells we have made the gate-source capacitance, C_{gs}, of the transconductors as large as possible while still allowing sufficient settling. Because the clock frequency of the system was set to 25 kHz these capacitors could be made as large as 4 pF. To reduce the effect of charge-injection and of clock-feed through we have used NMOS switches with dummy transistors.

The compensating subtraction and inverting of current signals are carried out with the use of current copiers as will be made clear in the next section.

The MAGFET interface

The output current from the MAGFET needs to be preprocessed before it is ready to be converted by the A/D – D/A system. In Fig. 8.7 the MAGFET and the preprocessing circuitry is shown. All switch control signals are supplied by the controlling finite state machine described later in this Chapter. In Mode 1 when the MAGFET offset current needs to be A/D converted and stored the current is simply sampled and held by the current copier, $\mathrm{CCOP_{sh}}$, and dumped directly into the A/D – D/A system. The MAGFET which utilizes

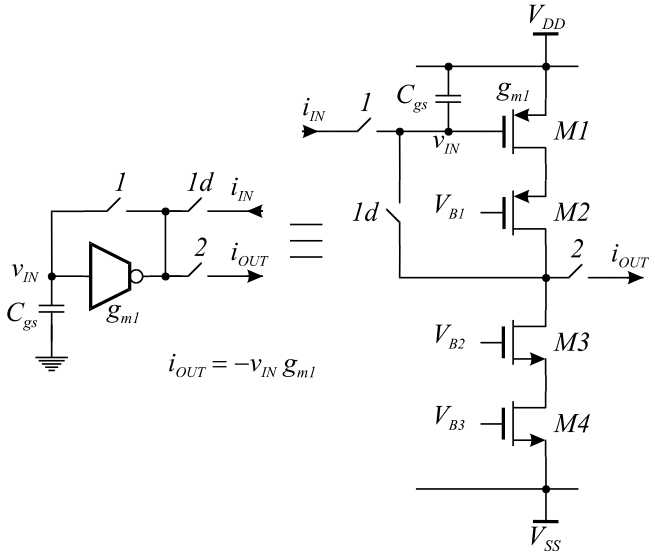

Figure 8.6: Diagram of the transconductor used in the current copier cells

120 μA bias current needs only to be turned on for a half clock period to be sampled in this way. This is important for lowering the supply current.

In Mode 2 when the MAGFET offset current needs to be out compensated the sampling scheme is a little different. First the digitally stored error is D/A converted and the result (which is the offset current with a change of sign) is present at the output of the accumulator (See Fig. 8.5). The current copier, $\mathrm{CCOP_{sh}}$, now samples and holds the MAGFET current subtracted by the D/A converted error signal, i.e. the MAGFET current and the output of the accumulator is both dumped into $\mathrm{CCOP_{sh}}$ and the result is held. If the value of the resulting current is positive the current is applied to the A/D – D/A system and the conversion will take place. If the sign of the current is negative the current is the dumped into the *sign changing* current copier, $\mathrm{CCOP_{sign}}$. On the next clock period the now positive current will be applied to the A/D – D/A system and the conversion will take place. This change of the sign of the current is necessary because the converter only can convert currents with a positive value. For determining the sign of the current the current comparator is used and the sign is registrated by the controlling unit for to determine the 3 MSB's.

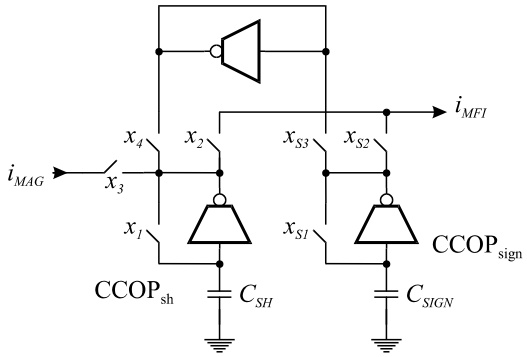

Figure 8.7: MAGFET interface

Staircase Generator

Fig. 8.8 shows a block diagram of the staircase generator. Its purpose is to generate a sequence of exponentially decaying current pulses that are accumulated in the accumulator. The staircase generator is build from three current copier's CCOP1, CCOP2, CCOP3 and a dummy load DL1. The staircase generator operates in the following way. On the first clock phase 1, the reference current, I_{REF}, is loaded into the current copier CCOP1 and the current in current copiers CCOP2 and CCOP3 is dumped to the dummy load and the accumulator respectively. These currents are not used in the first clock phase. On clock phase 2 the current in CCOP1 is loaded into CCOP2 and CCOP3. The current will be distributed between CCOP2 and CCOP3 depending on their transconductance ratios g_{m2} and g_{m3}. On clock phase 1 the current in CCOP2 is loaded into CCOP1 and the current in CCOP3 is sent to the accumulator. By continuing this it is obvious that the current leaving the staircase generator through CCOP3 will be given by: $I_{\text{stair}} = g_{m3}/g_{m2} \cdot I_{REF} \cdot (a, a^2, a^3, \ldots)$, where $a = g_{m2}/(g_{m2} + g_{m3})$. In this expression we have disregarded any errors in the current copier cells.

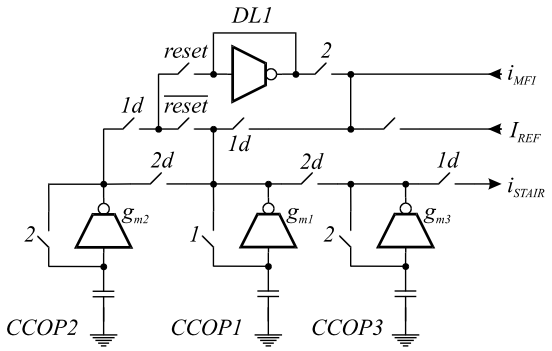

Figure 8.8: Block diagram of the staircase generator

Accumulator

Fig. 8.9 shows a block diagram of the accumulator. Its purpose is to accumulate the current pulses coming from the staircase generator. The accumulator is built from two current copiers, CCOP4 and CCOP5, and a dummy load DL2. The accumulator operates in the following way. On clock phase 1 the current pulse, $I_{ref} \cdot a^r$, enters the current copier CCOP4 and it comes out at the current output, i_{ACC}, with a value of $i_{ACC} = -(g_{m6}/g_{m5}) \cdot I_{REF} \cdot a^r$. On clock phase 2 the current in CCOP4 is either loaded into current copier CCOP5 or into the dummy load DL2, depending upon if it is to be accumulated or not. By continuing this operation for n clock periods it is possible to let the accumulator contain a given sum of current pulses.

Current Comparator

Fig. 8.10 shows a block diagram of the current comparator. Its purpose is to compare the input current, i_{IN}, against the contents of the accumulator, when the system is operating as a A/D converter. The comparison is performed by inverter INV1. On clock phase 2 the parasitic capacitors C_1, C_2 and C_3 are charged to the critical voltage of the inverter INV1. This implies that the node voltage at the switches S_1, S_2 and S_3 will be the same. This

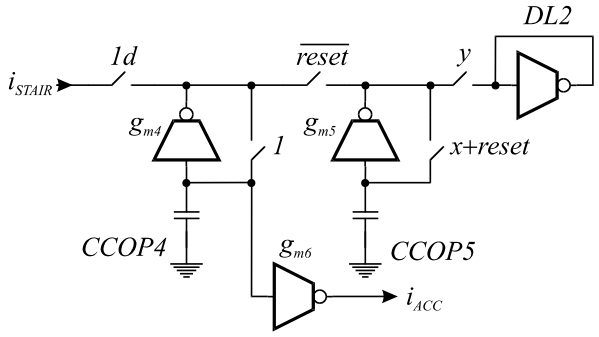

Figure 8.9: Block diagram of the accumulator

will result in good cancelling of charge injection from these switches. On clock phase 1 the current entering the current-comparator is used to charge the capacitor $C_1 + C_2$. Because the voltage on these capacitors already is identical to the critical voltage of the inverter INV1, it will respond very fast and its output will settle to either a high or low state. The output of INV1 is latched by the D–flip flop (D–FF) and shifted into the shift register.

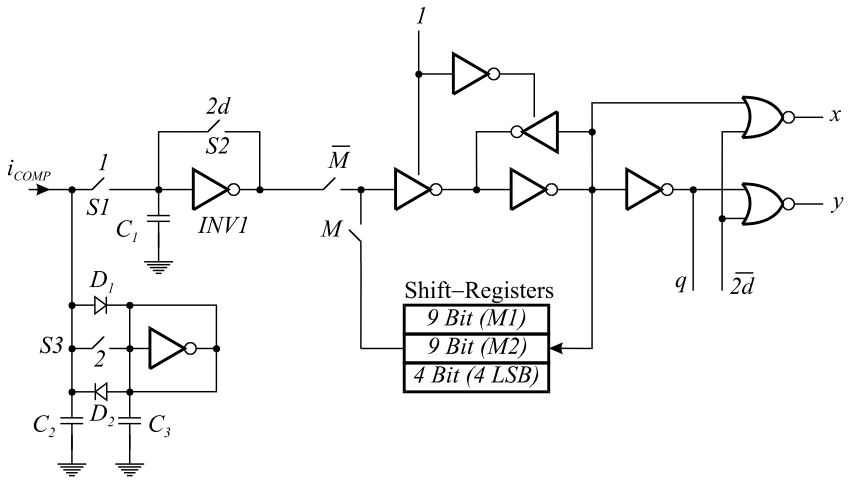

Figure 8.10: Block diagram of the current comparator

8.2.4 Digital Building Blocks

This Section contains a brief description of the implementation of digital circuitry used in the system. All circuitry was designed *in hand* and was optimized towards a minimum use of power.

Flip–Flops

All Flip–Flops are implemented with *tri–state logic* inverters. This implementation utilizes little area and have low power consumption as in transmission gate logic [35] but because the inputs are isolated from the switches (transmission gates) the required dynamic current delivery is greatly reduced.

Finite state machine

The system is controlled by a *finite state machine* (FSM) realized with the use of a *programmable logic array* (PLA) The PLA consists of two NOR planes controlled by a 5 bit counter and a 11 bit T–Flip–Flop (toggle flip–flop) latch register containing all controlling signals necessary for controlling the A/D – D/A system including the three MSB of the digital output. The FSM additionally controls the decoding of the digital output.

Clock Generator

Because a two phase nonoverlapping clock signal is crucial for correct operation of switched current circuitry a clock generator generating such a clock signal was designed (See Fig. 8.11). The square wave clock signal at the input (CLOCK) has been applied from an external clock generator. An internal clock oscillator capable of generating a square wave signal of 25 kHz will have to be designed

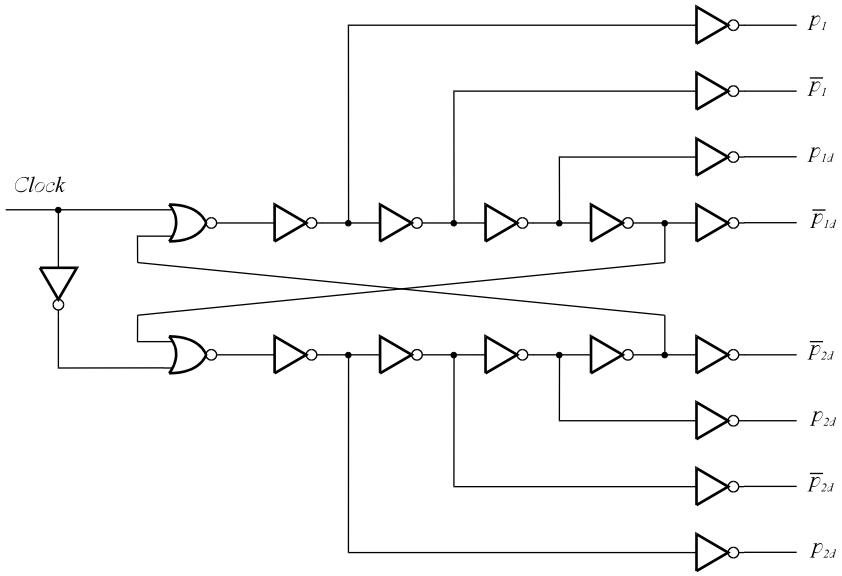

Figure 8.11: Two phase non-overlapping Clock generator

8.2.5 Error Analysis

In section 8.2.3 we showed that the output sequence of the staircase generator is given by: $I_{\text{stair}} = (g_{m3}/g_{m2}) \cdot I_{REF} \cdot (a, a^2, a^3, \ldots)$, where $a = g_{m2}/(g_{m2} + g_{m3})$ in the ideal case. But of course there will be some nonidealities in the staircase generator, i.e. finite ratio of g_o/g_m for the transconductor, that will tend to make $a = g_{m2}/(g_{m2} + g_{m3})$ slightly less than expected. There will also be some errors in the accumulator that will tend to make the accumulator lose some of its contents for every clock cycle. The impulse response sequence of the accumulator, if we regard it as a discrete time integrator, can therefore be represented by: $h_{acc} = (b, b^2, b^3, \ldots)$, were $b < 1$. The contents of the accumulator, while performing an A/D or D/A conversion, can therefore be viewed as the convolution of the output sequence of the staircase generator with the impulse response sequence of the accumulator. After n clock cycles the contents of the accumulator will therefore be given by:

$$\begin{aligned} i_{ACC} &= (g_{m3}/g_{m2}) \cdot I_{REF} \cdot (\mathrm{D1} \cdot a \cdot b^n + \mathrm{D2} \cdot a^2 \cdot b^{n-1} + \cdots \mathrm{Dn} \cdot a^n \cdot b) \\ &= (g_{m3}/g_{m2}) \cdot I_{REF} \cdot a \cdot b^n \cdot (\mathrm{D1} + \mathrm{D2} \cdot (a/b) + \cdots \mathrm{Dn} \cdot (a/b)^{n-1}) \\ &= k \cdot I_{REF} \cdot (\mathrm{D1} + \mathrm{D2} \cdot c + \cdots \mathrm{Dn} \cdot c^{n-1}) \end{aligned} \tag{8.2}$$

In the ideal case we would like to have $c = 0.5$, because it would result in a linear conversion. But because of the errors in the staircase generator and in the accumulator this will not be the case. To see how variations in c will influence the linearity of the D/A converter we will make use of Fig. 8.12 and Fig. 8.13. These two figures show the linearity of the D/A converter around changes in the MSB, where the errors are largest. The error

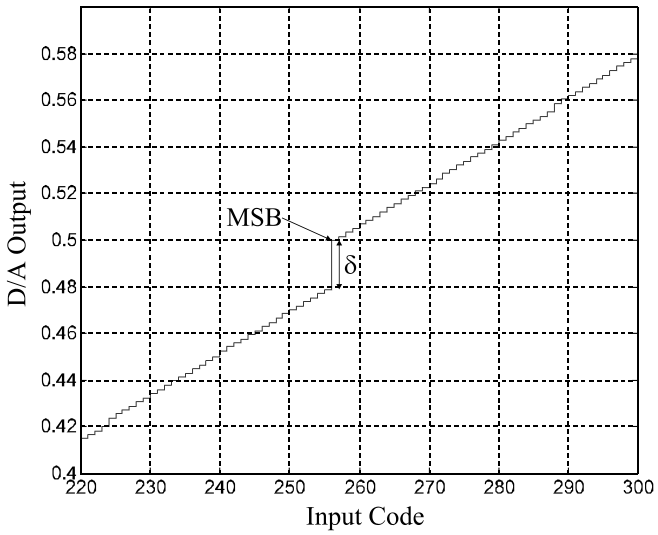

Figure 8.12: Linearity of D/A around MSB, with $c = 0.49$

when the MSB changes, i.e. a change from $(0111\ldots1)$ to $(1000\ldots0)$, is given by:

$$\delta = 1 - (c + c^2 + \cdots + c^{n-1}) = 1 - c\frac{1 - c^{n-1}}{1 - c} \tag{8.3}$$

As a start we will look at Fig. 8.12 where we have that $c < 0.5$. Let us now assume that we want to make a A/D conversion of a signal current that is slightly less than MSB. Because of the successive approximation algorithm the MSB will not be used and we will end up representing the signal by the sequence $(\mathrm{MSB}\ldots\mathrm{LSB}) = (0111\ldots1)$. Therefore the error between the A/D converted and the D/A converted signal can be as large as δ. Let us now look at Fig. 8.13 where we have that $c > 0.5$. And let us again assume that we want to make an A/D conversion of a signal current that is placed somewhere inside the range of δ. Now because of the successive approximation algorithm the MSB will be kept and some of the less significant bit's will be added to approximate the signal current. Therefore the error between the A/D converted and the D/A converted signal will be less than it was in the case where $c < 0.5$. If we consider all the error sources in the staircase generator and in the accumulator the relative accuracy of c will be in the range of $1\,\% - 2\,\%$. This implies that c should be in the range $0.499 < c < 0.545$ if we want to represent the signal current by 9 bit and if we allow the error between the A/D and D/A converted signal current to be less

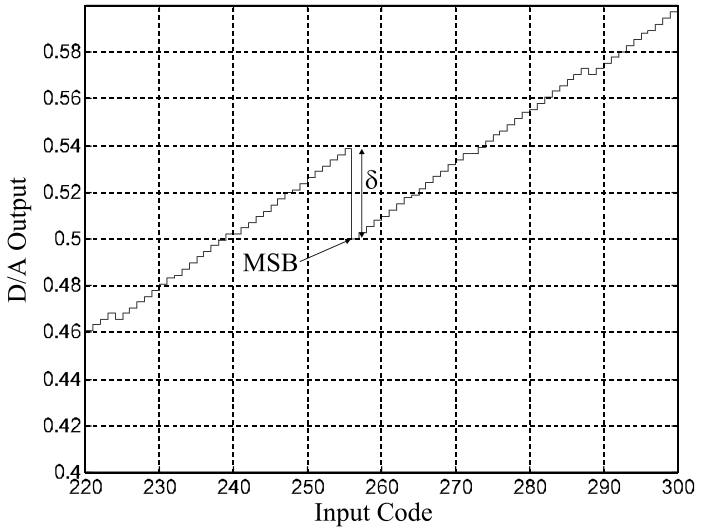

Figure 8.13: Linearity of D/A around MSB, with $c = 0.52$

than 2 LSB (this is equal to an accuracy of 8 bit). Because of this we chose $c = 0.52$ insuring that it will always be possible to perform a fairly accurate conversion of the signal current even when c should be 2 % less than expected i.e. $c = 0.51$. The dynamic range for our A/D – D/A conversion system, defined as the largest signal current divided by the smallest signal current, is given by:

$$\mathrm{DR} = \frac{I_{max}}{I_{min}} = \frac{1 + c^2 + \cdots + c^{n-1}}{c^{n-1}} = \frac{1 - c^{-n}}{1 - c^{-1}} \tag{8.4}$$

In our case with $c = 0.52$ we get $\mathrm{DR} = 388.6$ which equals 8.6 bit.

8.3 Layout

A test chip was implemented in an industry standard digital $1.5\mu m$ CMOS process (ES2). All of the Analog and the Digital building blocks were fully custom designed using the Layout editor L-Edit from Tanner Research.

A layout of the core of the MAGFET chip is shown in Fig. 8.14. This layout shows the main sections of the chip: The two MAGFET's, the serial A/D and D/A converter, Clock generator, Finite-State-Machine (FSM), and all of the Registers.

By using switched current techniques for the design of the serial A/D and D/A converter, we are able to integrate all of the A/D and D/A conversion circuitry with all of the digital circuitry on the same chip. This is a very important feature for making this a smart sensor concept.

8.4 Experimental Results

The circuit has been laid out in an industry standard 1.5μm CMOS process. The chip size is 2 mm × 2 mm and the circuitry uses approximately 60 % of this area. The reason for the chip size being this big is that it should fit to the bar magnet, which for practical reasons

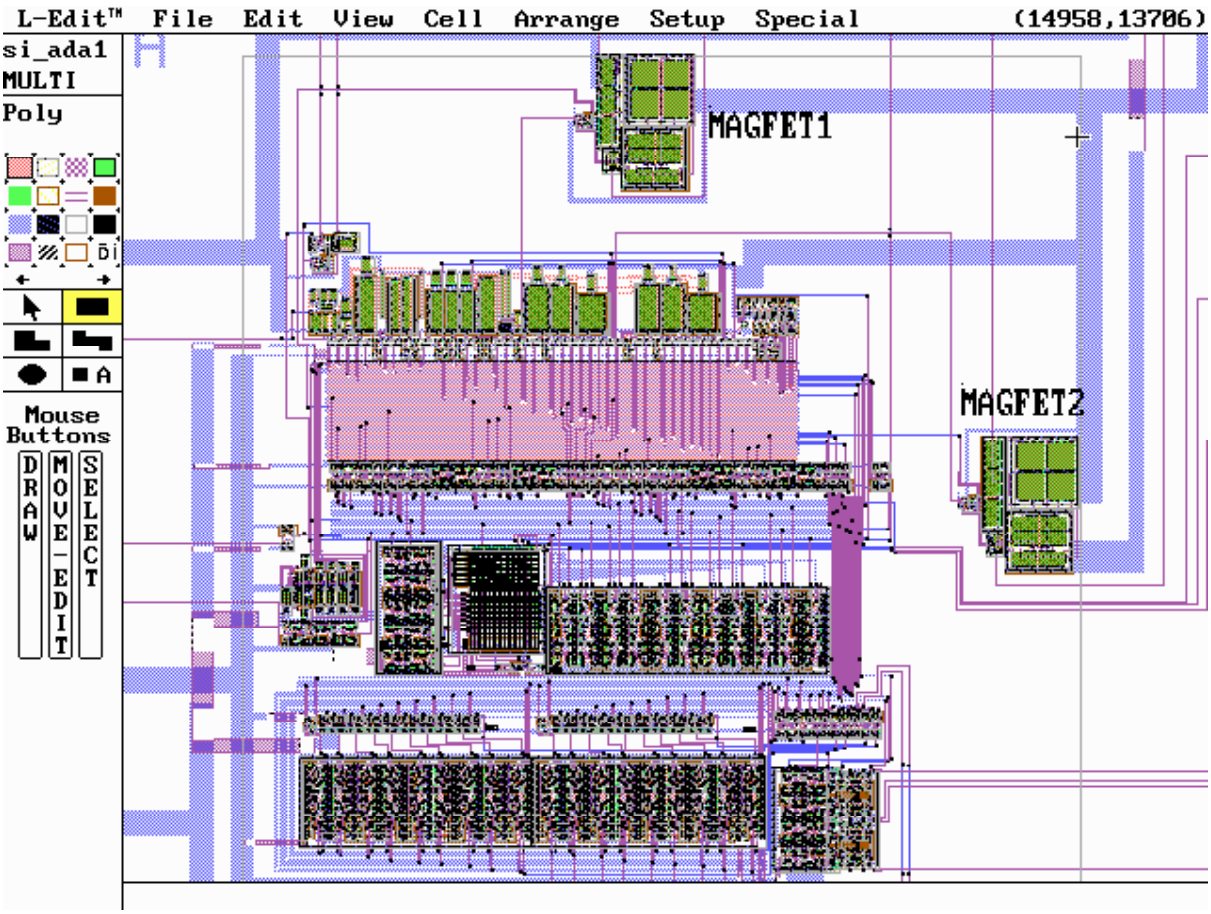

Figure 8.14: Layout of the core of the MAGFET chip

could not be made smaller. The dimensions of the bar magnet are 0.5 mm × 0.65 mm × 2 mm (HWL). The MAGFET will be exposed to a magnetic field in the range of ±0.25 T.

The electrical functionality of the A/D and D/A system has been verified by disabling the MAGFET currents and by applying some external signal currents into the system. In that way we were able to verify that the system was capable of performing offset compensations of the external signal currents. Also the system was able to perform both A/D and D/A conversions with a resolution of approximately 8 Bit's.

Measurements show that the system can operate with supply voltages down to 2.3 V. The current consumption of the switched current A/D – D/A conversion system is 38.5 μA and each MAGFET uses 120 μA. However, because of the small *turn on duty-cycle* the average current consumption is as low as 1.5 μA. The peak current , i.e. when the SI system and one of the MAGFET's are active at the same time, is close to 160 μA. The system operates correctly within the clock frequency range of 5 Hz to 25 kHz.

At the moment we are not able to measure the precise relationship between the angle of the bar magnet and the MAGFET output currents. This is due to an inadequate stability of the measurement setup.

8.5 Conclusion and Future Work

An angledetector with 7 bit digitally output has been described. It is meant as an alternative to the traditional slide potentiometer used as volume control in many hearing aids systems. Because of the absence of galvanic contact between the anglesetting device and the electrical circuitry the component is expected to increase lifetime of the component significantly.

One problem yet to be solved is to compensate for variations of the offset errors caused by temperature variations. Measurements have shown that there is a rather complex relationship between temperature and offset errors in the MAGFET's. At the time being this subject is investigated further.