# Chapter 9

# Switched Current Micropower 2nd Order Sigma-Delta A/D Converter

This chapter describes the design and implementation of a 2nd order Sigma-Delta A/D converter for low-power applications.

The reason for choosing Sigma-Delta Modulation for the A/D conversion is based on the fact that Sigma-Delta Modulators are very robust towards component mismatch i.e. the do not require precise matching of analog parts in order to achieve high resolution [37][38][39] ,in contrast to multibit A/D converters, where the resolution is determined by the accuracy of the matching of resistors, transistors e.t.c.

Also switched current techniques were chosen because of their compatibility with digital CMOS processes. The converter is implemented in a $0.6\mu m$ digital CMOS process with a single poly layer together with a large amount of digital circuitry.

The converter is designed to operate at supply voltages down to $3V$ with a supply current of $200\mu A$. It is implemented using fully differential class A switched current techniques resulting in a power consumption of $600\mu W$. The oversampling factor is $R = 128$ and the sampling frequency is 2.048MHz.

## 9.1 Design

The aim of this design was to achieve an A/D converter with a peak SNR of 72dB corresponding to a resolution of 12-bit's. With a traditional multibit converter this requires a matching in order of 0.025%, which can be very difficult to achieve in a digital CMOS process without trimming. Using Sigma-Delta Modulation, this resolution can be achieved without the need for trimming.

A SNR of 72dB is easily achieved with the second order Sigma-Delta modulator shown in Fig. 9.1. With an oversampling ratio of $R = 128$ this modulator has the potential of delivering an SNR of 85dB, which is sufficient for our purpose.

Because the Sigma-Delta modulator is implemented in switched current technique, it very important to minimize the internal signal swing in the integrators INT1 and INT2, in order to minimize the power consumption. A simulation showing the amplitude distribution of the internal signals in the integrators, of the modulator shown in Fig. 9.1, has been performed. The simulation was performed with a sine wave input signal with an amplitude of 0.85 and a normalized frequency of 1/512. The results of this simulation are shown in Fig. 9.2.

This simulation shows that integrator INT2 has approximately twice the internal signal swing of integrator INT1. The internal signal swing in integrator INT2 can however easily be

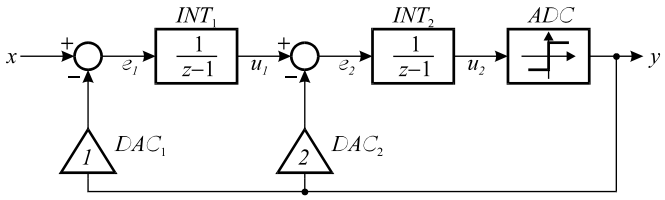


Figure 9.1: Basic Sigma-Delta Modulator

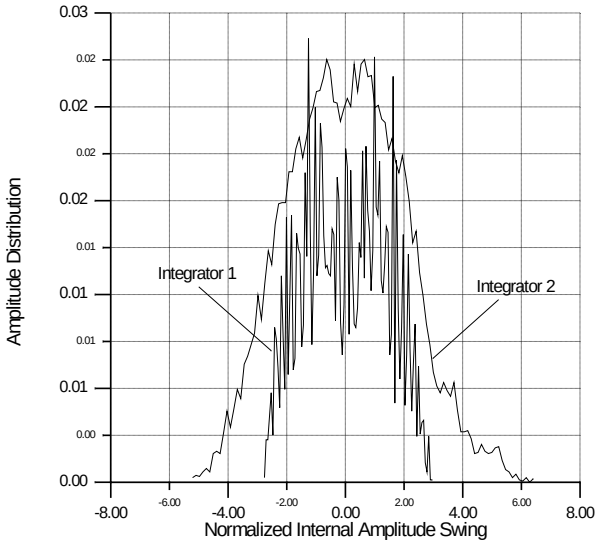


Figure 9.2: Amplitude distribution of internal signal swing in the integrators for the basic sigma-delta modulator

reduced by a factor of two by scaling all of the input branches to the input of the integrator by a factor 0.5. At the same time we increase the gain of integrator INT2 by a factor two in order maintain the overall loop gain.

In Fig. 9.1 integrator INT2 is followed by a 1-bit ADC (Comparator) which only looks at the sign of the signal, therefore the gain of integrator INT2 is of no importance to the modulator, because it is absorbed into the ADC. The effect of this is that the gain of integrator INT2 can arbitrarily be chosen to one as shown in Fig. 9.3.

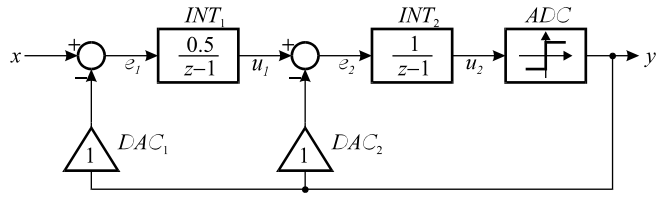


Figure 9.3: Modified Sigma-Delta Modulator, for reduced internal signal swing

A simulation showing the amplitude distribution of the internal signals in the integrators of the modulator shown in Fig. 9.3, has been performed. The simulation was performed with a sine input signal with an amplitude of 0.85 and a normalized frequency of 1/512. The

results of this simulation are shown in Fig. 9.4.

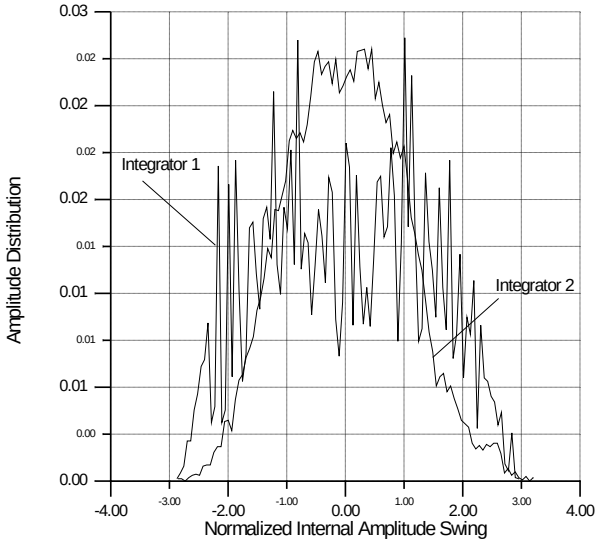


Figure 9.4: Amplitude distribution of internal signal swing in the integrators for the modified sigma-delta modulator

This simulation shows that integrator INT2 now as approximately the same internal signal swing as integrator INT1 after we have scaled the modulator filter.

For the modulator shown in Fig. 9.3, a simulation showing the SNR as a function of input amplitude has been performed. The results of this simulation are shown in Fig. 9.5. This simulation shows that the modulator has the potential of delivering a SNR of 85dB with an normalized input amplitude of 0.85. For input amplitudes larger than 0.85 the SNR is suddenly reduced, this indicates the onset of instability.

## 9.2 Implementation

The Sigma-Delta modulator designed in this chapter is based on the topology shown in Fig. 9.3. Before we begin the design of the modulator, it is of great importance to know which sections of the modulator are the critical ones.

Any nonlinearities and noise generated in DAC2 and INT2 are noise shaped by the modulator itself, reducing the influence of these errors far below that of DAC1 and INT1. This is easily verified by considering the transfer function from the input of integrator INT2 to the modulator output compared to the transfer function from the input of integrator INT1 to the output of the modulator. The ratio between these two transfer functions is given by $(1-z^{-1})$ indicating that any errors in integrator INT2 and DAC2 are suppressed at low frequencies. Therefore any errors in DAC1 and INT1 will be the limiting factor of the performance of the Sigma-Delta modulator.

Simulations have shown that any clipping of the internal signals in integrator INT1 will produce tones at the output of the Sigma-Delta modulator. In order to avoid this, the integrator INT1 has been designed so that it is capable of handling larger internal signals than shown in Fig. 9.4. We have chosen to design INT1 so that it can handle internal signals that are four times larger than the full scale input signal.

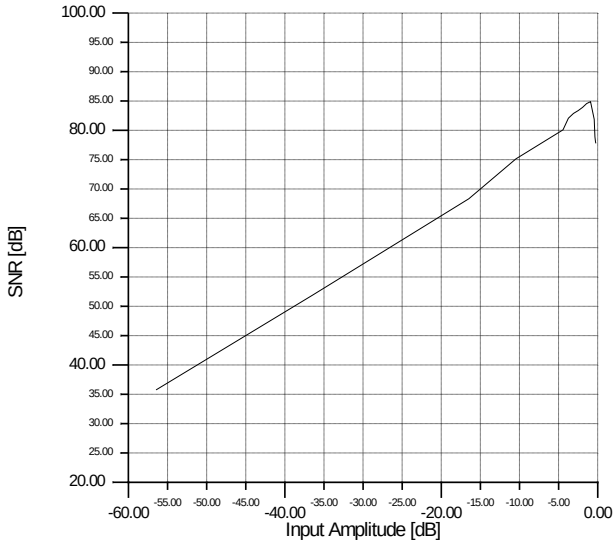


Figure 9.5: SNR for different input amplitudes at the input of the modulator

The Sigma-Delta modulator is to be implemented in a digital $0.6\mu m$ CMOS process together with a large amount of digital circuitry. To minimize the noise coupling from the digital circuitry into the A/D converter we choose to implement it using fully differential switched current techniques. A block diagram of the sigma-delta modulator is shown in Fig. 9.6.

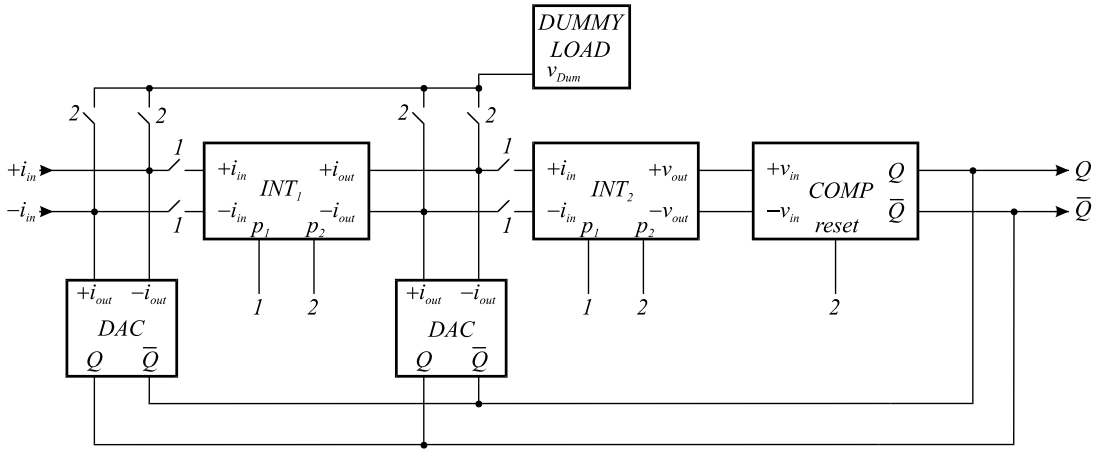


Figure 9.6: Block diagram of the fully differential 2nd order sigma-delta modulator

### 9.2.1 DAC's

One of the greatest advantages inherited in using 1-Bit DAC's is that there are no nonlinearity errors. We only observe linear errors i.e. scaling and offset errors, this fact reduces the demands on the DAC, considerably.

A simple current steering DAC has been used in this design, and it is shown in Fig. 9.7. The DAC consist basically of a current source M1 and a differential pair M2,M3 operating

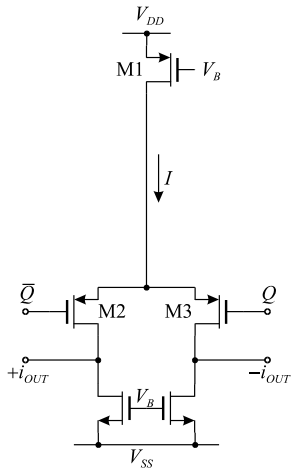


Figure 9.7: 1-Bit DAC

as a current switch. The current $I$ from the current source M1 corresponds to the full scale signal current entering the Sigma-Delta modulator.

### 9.2.2 Integrators

The integrators used in this design are based on the Cascode II structure, described in Chapter 2. The critical part of the Sigma-Delta modulator is the first integrator because it determines the SNR and the linearity. Therefore the main design effort is put into the first integrator.

The two integrators INT1 and INT2 are different, the first integrator has a current output with a scaling factor of 0.5 and the second integrator has a voltage output, feeding the voltage comparator (1-bit ADC), and with an arbitrary scaling factor.

#### Integrator 1

A circuit diagram, showing the integrator INT1 together with DAC1, is shown in Fig. 9.8. The

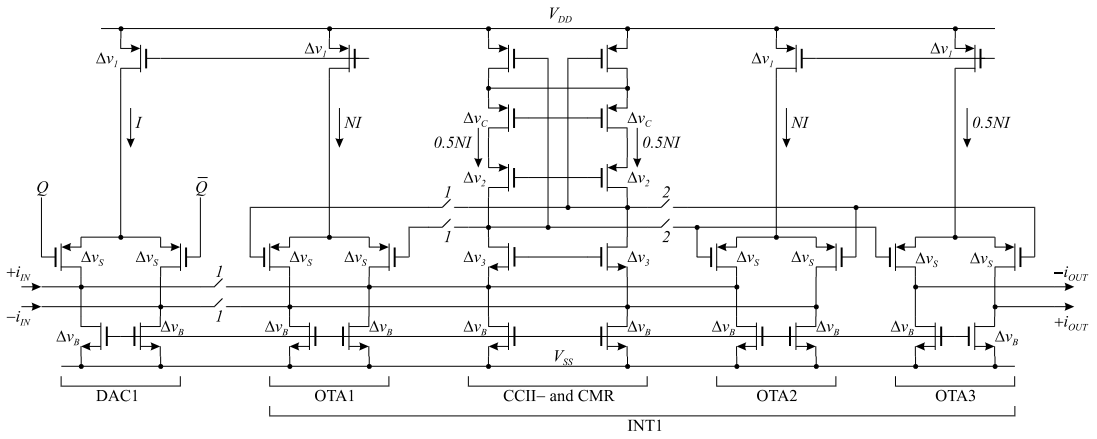


Figure 9.8: Integrator INT1 and DAC1

integrator core consists of the two fully differential transconductors OTA1 and OTA2 together

with the fully differential folded cascode current conveyor CCII−, that also incorporates a commonmode feedback regulation CMR. The current conveyor is based on a folded cascode structure, and the commonmode regulation is based on a source degenerated current source. The current conveyor and the commonmode regulation used in this design is described in Chapter 2.

In order to get the required scaling factor of 0.5 for the integrator, an output transconductor OTA3 is connected to the transconductor OTA2. The transconductors OTA2 and OTA3 effectively operate as a fully differential current mirror with a scaling factor of 0.5.

We have previously shown that the modulator structure has the potential for delivering a peak SNR of 85dB at an oversampling factor of $R = 128$. Our requirements are a SNR of 72dB corresponding to 12-Bit i.e. we have an overhead of 13dB. This overhead can be used to reduce the power consumption of the Sigma-Delta modulator, by designing the first integrator INT1 so that it is the thermal noise from this integrator that limits the SNR to 72dB.

**Calculation of the SNR for the Sigma-Delta modulator:** The SNR of the Sigma-Delta modulator is limited by the noise from DAC1, OTA1,OTA2 the CCII− and the CMR. In our noise analysis, we will only consider thermal white noise generated in the MOS transistors. The reason for this is that all of the low frequency $1/f$ noise generated in the integrator is exposed to correlated double sampling CDS, which reduces the effect of this noise far below the thermal white noise (see Chapter 5).

This is however not true for the low frequency $1/f$ noise generated in DAC1 because the DAC is only connected to the integrator on clock phase 1. In order to get CDS it is necessary for the DAC1 to be connected to the integrator on both clock phase 1 and 2 (see Chapter 10).

Even though we might expect to get some low frequency $1/f$ noise from DAC1 we will ignore that in our noise analysis.

In Fig. 9.8, all of the PMOS transistors whose source is tied directly to the supply voltage $V_{DD}$ do not contribute with any significant noise to the integrator. This is because the noise from these transistors is mostly commonmode noise as can be seen from the figure.

This is however not the whole truth for the noise from the PMOS transistors in the OTA's. Because of the large differential signal swings at the input of the differential pairs in the OTA's, the noise generated in the tail current source will increasingly be turned into a differential component at the output of the differential pair, leading to increased noise at the output of the OTA.

Normally, in operational amplifiers this behavior is not seen because the differential pair in the input of the operational pair is not exposed to large differential signals because of the feedback around the op-amp (virtual ground).

All of the other transistors shown in the figure contribute with noise that we have to take into account, when calculating the noise power.

All of the noisy MOS transistors have a corresponding power spectral density $S_{in}^{w}$, that can be represented as

$$S_{in}^{w} = 2kT\frac{2}{3}g_m \tag{9.1}$$

The power spectral density at the input of the integrator can be found as the sum of all of these contributions

$$S_{in,e}^{w} = 2kT\frac{2}{3}\sum g_m \tag{9.2}$$

where $\sum g_m$ is the equivalent input transconductance. From Fig. 9.8 we get the following

contributions to the equivalent input transconductance.

$$\begin{aligned} \text{DAC1} &: g_m = 2(g_{ms} + g_{mb}) && (9.3)\\ \text{OTA1,OTA2} &: g_m = 2 \cdot 2 \cdot 2N(g_{ms} + g_{mb}) && (9.4)\\ \text{CCII}-\text{, CMR} &: g_m = 2 \cdot 2N(g_{mc} + g_{mb}) && (9.5) \end{aligned}$$

The total equivalent input transconductance is therefore

$$\sum g_m = 2\left[g_{ms}(4N+1) + g_{mb}(6N+1) + g_{mc}2N\right] \tag{9.6}$$

giving a equivalent input power spectral density

$$S^w_{in,e} = 2kT\frac{4}{3}g_{ms}\left[(4N+1) + (6N+1)\frac{g_{mb}}{g_{ms}} + 2N\frac{g_{mc}}{g_{ms}}\right] \tag{9.7}$$

Assuming that the bandwidth of the current copiers formed by OTA1 and OTA2 is the same, we get that the power spectrum of the sampled analog noise is given by (see Appendix E)

$$\begin{aligned} s^w_{in.e} &= S^w_{in,e}\frac{g_{ms}}{2C} && (9.8)\\ &= \frac{kT}{C}\frac{4}{3}g^2_{ms}\left[(4N+1) + (6N+1)\frac{g_{mb}}{g_{ms}} + 2N\frac{g_{mc}}{g_{ms}}\right] && (9.9) \end{aligned}$$

The noise power at the input of the Sigma-Delta modulator can now be found by integrating the equivalent input noise power spectrum over the frequency range of interest.

$$P_{in,e} = \frac{1}{f_s}\int_{-f_b}^{+f_b} s^w_{in.e}df = s^w_{in.e}\frac{2f_b}{f_s} = s^w_{in.e}\frac{2\frac{f_s}{2R}}{f_s} = s^w_{in.e}\frac{1}{R} \tag{9.10}$$

This equation shows that the noise power is reduced by the oversampling factor $R$.

Assuming that the amplitude of the input signal current is a fraction $m$ of the bias current $I$, the power of the input signal current entering the Sigma-Delta modulator is given by

$$P_s = \frac{m^2I^2}{2} \tag{9.11}$$

The signal-to-noise-ratio SNR at the input of the Sigma-Delta modulator is therefore given by

$$\begin{aligned} SNR &= \frac{P_s}{P_{in,e}} && (9.12)\\ &= R\frac{m^2I^2}{\frac{kT}{C}\frac{8}{3}g^2_{ms}\left[(4N+1) + (6N+1)\frac{g_{mb}}{g_{ms}} + 2N\frac{g_{mc}}{g_{ms}}\right]} && (9.13)\\ &= m^2RC\frac{\Delta v_s^2}{kT\frac{8}{3}\left[(4N+1) + (6N+1)\frac{\Delta v_s}{\Delta v_b} + 2N\frac{\Delta v_s}{\Delta v_c}\right]} && (9.14) \end{aligned}$$

This equation shows that an large internal dynamic range $N$ will reduce the SNR unless the storage capacitance $C$ is increased accordingly which of course implies that the supply current must be increased to keep up the settling properties.

The first integrator INT1 was optimized for minimum storage capacitance $C$ with a fixed modulation index $m$ and an internal dynamic range $N$ equal to $N = 4$. The optimization gave the saturation voltages and the storage capacitance shown in Table 9.1

Table 9.1: Saturation voltages and storage capacitance found for the Sigma-Delta modulator

| *Parameter* | *Value* |
|---|---|
| $\Delta v_s$ | 0.75V |
| $\Delta v_b$ | 0.55V |
| $\Delta v_c$ | 0.7V |
| $\Delta v_1$ | 0.2V |
| $\Delta v_2$ | 0.3V |
| $\Delta v_3$ | 0.1V |
| $C$ | 0.15pF |
| $V_{CM}$ | 1.86V |

The only parameter missing is the bias current $I$, which is determined by the settling properties of the integrator (see Chapter 4 and Chapter 5). We choose the small signal settling error of $\epsilon = 0.1\%$, which corresponds to a bias current equal to $I = 3.15\mu A$. Based on this the bias current was chosen to $\underline{I = 5\mu A}$.

All of the other circuit blocks in the sigma-delta modulator use the same saturation voltages as shown in Table 9.1 and the same unit current $I = 5\mu A$.

### Integrator 2

The less critical integrator INT2 is shown in Fig. 9.9. This figure shows that this integrator is build in the same way as the first integrator INT1 with the exception of a missing output transconductor because we have no need for a specific scaling in this integrator. This is due to the comparator (1-bir ADC). The integrator is designed using the same parameters as

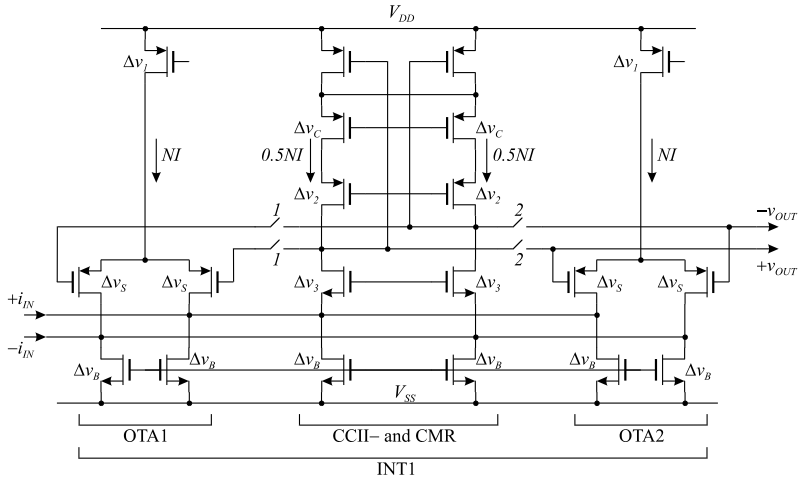


Figure 9.9: Integrator INT2

shown in Table 9.1 and with an internal dynamic range of $N = 3$.

### 9.2.3 Comparator

The 1-Bit ADC (Comparator) used in the Sigma-Delta modulator is based on a regenerative comparator using positive feedback scheme, in order to obtain fast response time. The circuit diagram of this voltage comparator is shown in Fig. 9.10.

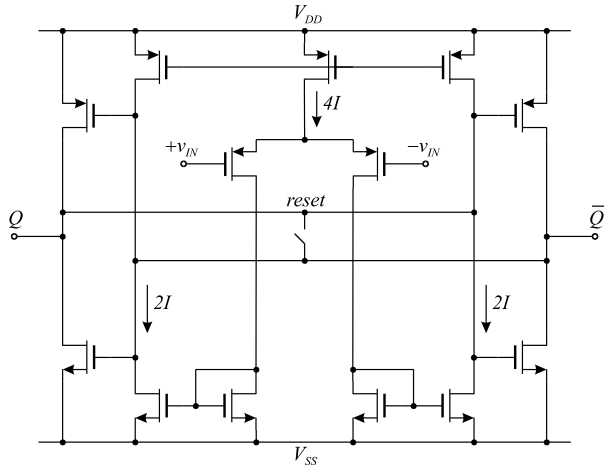


Figure 9.10: Fully differential regenerative voltage Comparator

## 9.3 Experimental Results

The design of this Sigma-Delta Modulator was done for a second part, that was responsible for doing the actual layout of the Sigma-Delta modulator and for performing test on the fabricated chip. Unfortunately, at the moment I have no layout of the chip and no available experimental results to report.

## 9.4 Conclusion and Future Work

This design example has shown an application of switched current techniques for implementing low power Sigma-Delta A/D converters.

An approximate estimate of the supply current is found to be:

**DAC1,DAC2 :** $I + I = 2I$

**INT1 :** $4I + 4I + 4I + 2I = 14I$

**INT2 :** $14I \cdot \frac{3}{4} = 10.5I$

**ADC :** $2I + 4I + 2I = 8I$

giving a total supply current of $Isup \simeq 34.5I = 34.5 \cdot 5\mu A = 172.5\mu A$. If we take into account the supply current used by the bias circuitry, the dummy load and the clock generator, we end up with a supply current of $\underline{Isup \simeq 200\mu A}$. Operating at a supply voltage of $\underline{Vsup = 3V}$, this gives a power consumption of $\underline{Psup \simeq 600\mu W}$.

We have previously shown that the SNR could be written as

$$SNR \simeq \frac{m^2}{N} RC \frac{\Delta v_s^2}{kT\frac{4}{3}\left[4 + 6\frac{\Delta v_s}{\Delta v_b} + 2\frac{\Delta v_s}{\Delta v_c}\right]} \tag{9.15}$$

from this equation we can conclude that for a given SNR, the power consumption is independent of the oversampling ratio $R$. This can be reasoned as follows: If we increase the oversampling factor $R$ by some amount, we can decrease the storage capacitance with the same amount and still maintain our SNR. When we increase the oversampling factor $R$ we must also increase the bandwidth of the switched current circuits in order to maintain the settling behavior, but this is automatically fulfilled as we have decreased the storage capacitance $C$. Therefore the *supply current is independent of the oversampling factor $R$ for a given SNR.*

The consequence of this is that the power consumption is not determined by the operating speed (sampling frequency), but by the signal-to-noise-ratio SNR.

Each time we increase the SNR by 6dB we have to increase the storage capacitance by a factor four. To maintain the settling behavior, we therefore have to increase the supply current by a factor four, leading to a four times increase of the power consumption. Therefore a large SNR is very expensive in terms of power consumption.